VL82C320

SYSTEM CONTROLLER/DATA BUFFER

DESCRIPTION

The VL82C320 contains the system control and data buffering functions in a 160-lead quad flat pack.

The VL82C320's functions are highly programmable via a set of internal configuration registers. Defaults on reset for the configuration registers allow the system to boot at the CPU's rated speed. However, operational capabilities may be temporarily reduced until the configuration registers are set to mirror the true system configuration. This normally is a function of BIOS setup.

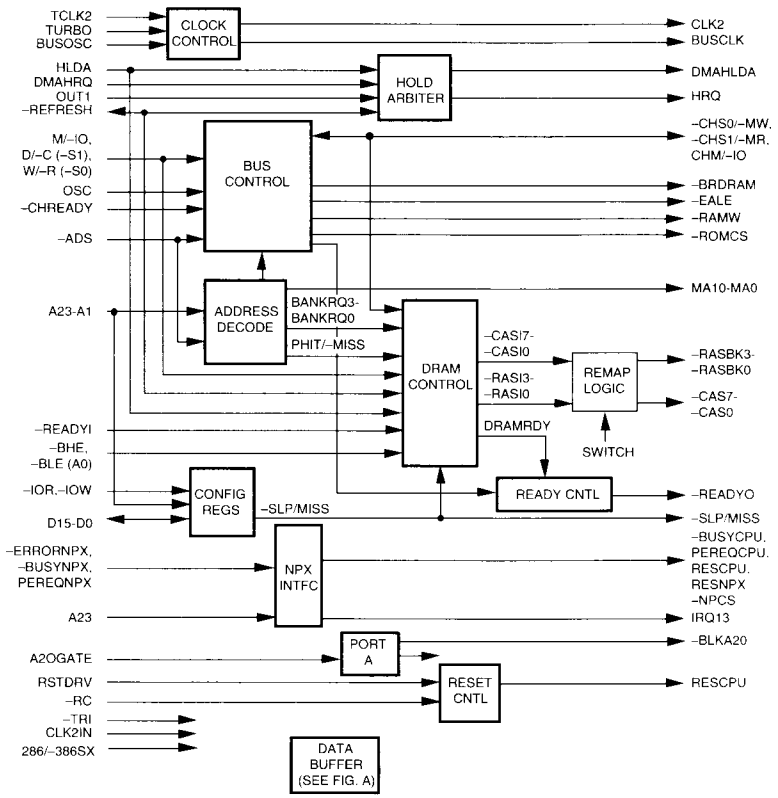
The VL82C320 is designed to perform in systems running up to 20 MHz. Built-in page mode operation, two- or four-way interleaving, and fully programmable memory timing allow the PC designer to maximize system performance using commodity DRAMs. Programmable memory timing allows the system to be setup to match the requirements of the chosen DRAMs; standard or custom.

The System Controller handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the VL82C331 ISA Bus Controller. The refresh rate is programmable to submultiples of 15 ms. This allows use of low-power, slow refresh DRAMs. The VL82C320 controls all timing in both modes. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the VDD and ground pins. In sleep mode, –CAS before –RAS refresh may be switched for maximum power savings.

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are convenient. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function performs this task by switching the internal –RASBK and CAS signals between the external –RASBK and CAS pins. This allows internal row and column address strobes generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

4

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C320-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

The Intel 287™ numeric coprocessor is supported when the VL82C320 is strapped for 286 mode. When strapped for 386SX mode, the 387™SX is supported. Support is for both 8-bit wide and 16-bit wide system BIOS ROM.

EEMS support is provided in hardware for the complete LIM EMS 4.0® standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill down to 256K for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to EFFFFh. These twelve registers can alternatively be mapped in the A0000-BFFFFh and D0000h-DFFFFh range by changing a configuration bit in the VL82C320. All registers are capable of translating over the complete 32 Mbyte range of on-board DRAM. Users preferring an alternate plug-in EMS solution, can disable the on-board EMS system as well as system board DRAM, as required, down to 256K.

Shadowing features are supported on all 16K boundaries between 640K and 1M. Simultaneous EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided.

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

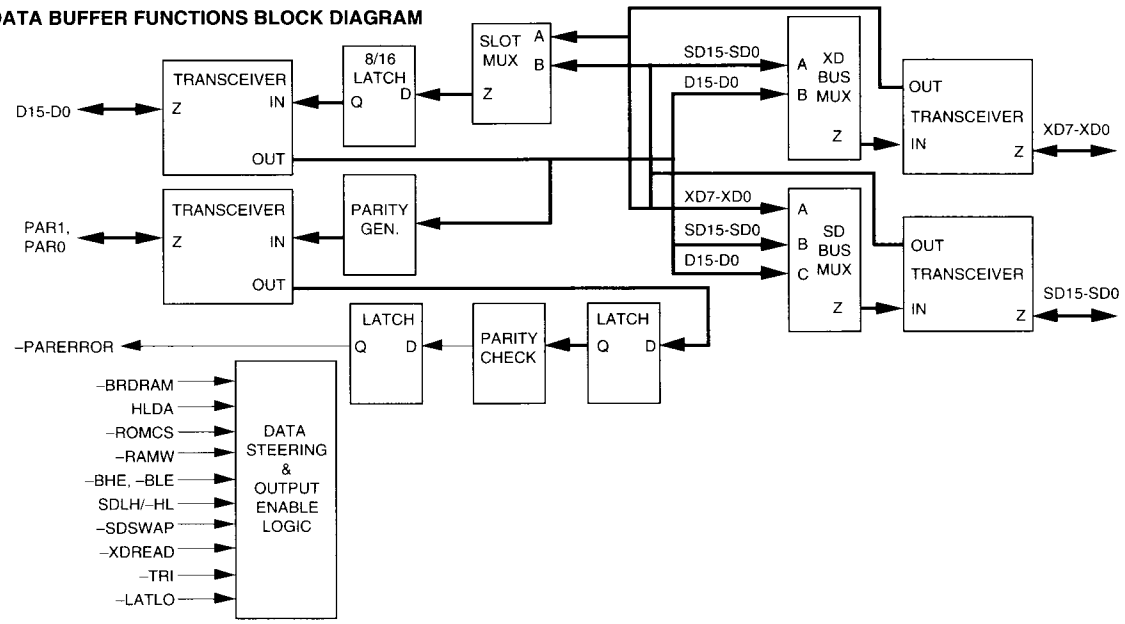
These controls are overridden by EMS in segments for which it is enabled.

The VL82C320 is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller. The bus clock may be derived from the TCLK2 or bus OSC inputs. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3, or 4.

The VL82C320 also performs all of the data buffering functions required for a 286- or 386SX-based PC/AT®-compatible system. Under the control of the CPU, the data buffer chip routes data to and from the CPU's D bus, XD bus, and slots (SD bus). The parity is checked for D bus DRAM read operations and generated for D bus DRAM write operations. The VL82C320 provides the data conversion necessary for 16-bit accesses to 8-bit devices on the XD or SD buses. The data is latched for synchronization with the CPU.

Under the control of DMA or a Bus Master, the VL82C320 allows 8- or 16-bit data to be routed to and from the XD bus. The chip also is capable of performing high-to-low and low-to-high byte swaps on the SD bus. The chip also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

DATA BUFFER FUNCTIONS BLOCK DIAGRAM



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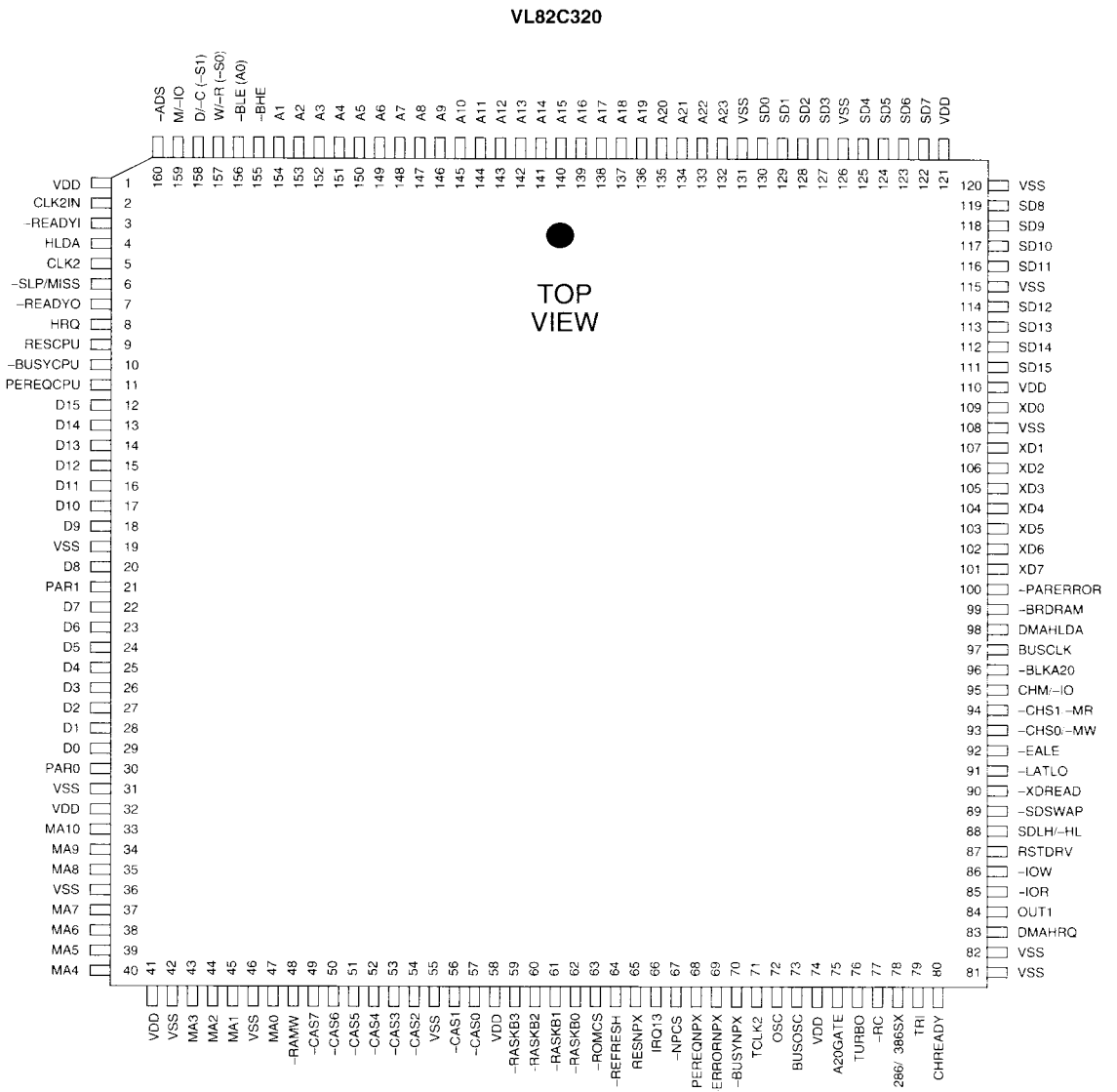
PIN DIAGRAM



Note: Parenthesis indicate 286 pin functions.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A23-A1	132-154	I-TTL	Address bits 23 through 1 - When the CPU is Bus Master and HLDA is active, these signals are driven by the Bus Controller.
–BHE	155	I-TTL	Byte High Enable, active low - This signal is driven by the CPU or the Bus Controller. It is used to select the upper byte of a 16-bit wide memory location.
–BLE (A0)	156	I-TTL	Byte Low Enable, active low, or A0 - In 386SX mode this signal is –BLE, in 286 mode it is A0 and is driven by the CPU or the Bus Controller. It is used to select the lower byte of a 16-bit wide memory location.
W/–R (–S0)	157	I-TPU	Write or active low Read enable, or S0 - This is W/–R in 386SX mode or –S0 in 286 mode. This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.
D/–C (–S1)	158	I-TPU	Data or active low Code enable, or S1 - D/–C is driven by the CPU in 386SX mode or –S1 in 286 mode. This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.
M/–IO	159	I-TPU	Memory or active low I/O enable - M/–IO is decoded with the remaining control signals to indicate the type of bus cycle requested.
–ADS	160	I-TPU	Address Strobe, active low - This signal is driven by the 386SX as an indicator that the address and control signals are valid. It is used internally to indicate that the address and command are valid and determine the beginning of a bus cycle. This pin is a "no connect" in 286 mode.
CLK2IN	2	I-CMOS	This is the main clock input to the VL82C320 and it should be connected to the CLK2 signal that is output by the VL82C320. This signal is used internally to clock the VL82C320 logic.
TCLK2	71	I-CMOS	This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The CMOS level is used to generate CLK2 output and optionally, bus clock.
CLK2	5	O	This output signal is CMOS level and generated from TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
–SLP/MISS	6	IT-OD	As a "power-on reset" default, this signal is an output that is equal to –SLEEP7 • –SLEEP1. When configuration register CTRL0 = 1, this pin becomes a MISS input for use with a future VLSI product.
–READYO	7	O	Ready Out, active low - This signal is an indication that the current cycle is complete. It is generated from the internal DRAM Controller or the synchronized version of –CHREADY for slot bus accesses. The culmination of these ORed READY signals is sent to the CPU and is also connected to the VL82C320's –READYI input. This signal may be combined externally with other READY sources.
–READYI	3	I-TTL	Ready Input, active low - This signal indicates the current bus cycle is complete.
HLDA	4	I-TTL	Hold Acknowledge, active high - This signal is issued in response to the HRQ driven by the VL82C320. When HLDA is active, the memory control is generated from –CHS1/–MR and –CHS0/–MW.
HRQ	8	O	Hold Request, active high - This signal indicates that a Bus Master, such as a DMA or AT Channel Master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a refresh cycle. It is synchronized to CLK2 and internal clock.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
RESCPU	9	O	Reset CPU, active high - This signal is issued in response to the control bit for software reset located in the Port A, read from I/O port EFh, RC and RSTDRV inputs and in response to VL82C320's detection of a shutdown command. In all cases it is synchronized to CLK2 and internal clock.
–BUSYCPU	10	O	Busy CPU, active low - The state of –BUSYNPX is always passed through to –BUSYCPU indicating that the NPX is processing a command. On occurrence of an –ERRORNPX signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RSTDRV.
PEREQCPU	11	O	Processor Extension Request CPU, active high - An output signal generated in response to a PEREQNPX which is issued by the coprocessor to the VL82C320. PEREQCPU is asserted on occurrence of –ERRORNPX after –BUSYNPX has gone inactive. A write to F0h returns control of the PEREQCPU signal to directly follow the PEREQNPX input. This is used only in 386SX systems. It is a "no connect" in 286-based systems.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
–RAMW	48	O-TTL	RAM Write, active low - This signal is active during memory write cycles and high at all other times.
MA10-MA0	33-35, 37-40, 43-45, 47	O-TTL	Memory Addresses bits 10 through 0 - These address bits are the row and and column addresses sent to on-board memory. They are buffered and multiplexed versions of the CPU bus addresses.
–RASBK3 - –RASBK0	59-62	O-TTL	Row Address Strobe, active low - These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is fully programmable.
–CAS7 - –CAS0	49-54, 56, 57	O	Column Address, Strobe, active low - These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a –CAS signal for the upper and lower bytes of each of the four 16-bit DRAM memory banks. The active period for this signal is completely programmable. For clarity, alternate names may also be used for these signals as shown in the following table where the digit in the "Alternate Name" indicates the DRAM bank the signal drives, L indicates it drives the low byte, and H indicates it drives the high byte.
–REFRESH	64	IC-OD	Refresh signal, active low - This output is used by the VL82C320 to initiate an off-board DRAM refresh operation.
–ROMCS	63	O	ROM Chip Select - This is the on-board system BIOS ROM chip select.
COPROCESSOR SIGNALS			
PEREQNPX	68	I-TPD	Coprocessor Extension Request NPX, active high - This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts. This is used only in 386SX systems. It is a "no connect" in 286-based systems.

Standard Name	Alternate Name
–CAS0	–CAS0L
–CAS1	–CAS0H
–CAS2	–CAS1L
–CAS3	–CAS1H
–CAS4	–CAS2L
–CAS5	–CAS2H
–CAS6	–CAS3L
–CAS7	–CAS3H

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ERRORNPX	69	I-TPU	Error NPX, active low - An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with –BUSYNPX to produce IRQ13.
–BUSYNPX	70	I-TPU	Busy NPX, active low - An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQCPU.
RESNPX	65	O	Reset NPX - This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. Write to port F1h only resets the coprocessor. A software FINIT signal must occur after an F1h generated reset in a 386SX-based system, otherwise, the 387SX is not initialized to the same state that a 287 is placed in by a hardware reset alone. Optionally, the F1 reset may be disabled by setting bit 6 of the MISCSET register to 1.
IRQ13	66	O	Interrupt Request, active high - This output is driven to the Bus Controller to indicate that an error has occurred within the coprocessor. This signal is a decode of the –BUSYNPX and –ERRORNPX inputs.
–NPCS	67	O	Coprocessor Chip Select - Provides decoding of the 287 coprocessor's I/O space. This is the entire F8h to FFh region when Special Features are disabled. When Special Features are enabled, only I/O accesses to F8h, FAh, FCh, and FEh cause –NPCS to be active. This signal is a "no connect" pin for 387SX operation, and reserved for future use in 386SX-based systems.
BUS CONTROL SIGNALS			
–CHREADY	80	I-CMOS	Channel Ready, active low - An input issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with READY signals from the coprocessor and DRAM Controller to form the final version of –READYO which is sent to the CPU.
–CHS0/–MW	93	IO-CMOS	Channel Select 0 or Memory Write, active low - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS1 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMW signal for the DMA or Bus Master to access system memory.
–CHS1/–MR	94	IO-CMOS	Channel Select 1 or Memory Read, active low - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for the DMA or Bus Master to access system memory.
CHM/–IO	95	O	Channel Memory I/O - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHS1 and decoded, the bus cycle type is defined for the Bus Controller.
–BLKA20	96	O	Block A20, active low - An output driven to the Bus Controller to deactivate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 Mbyte memory boundary. Port A bit 1 may be directly written or set by a read of I/O port EEh.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUSOSC	73	I-TTL	Bus Oscillator - This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the VL82C320's internal configuration registers are set for asynchronous slot bus mode.
BUSCLK	97	O	Bus Clock - This is the source clock used by the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is a programmable division from TCLK2 or BUSOSC.
DMAHRQ	83	I-CMOS	DMA Hold Request, active high - This signal is an input sent by the Bus Controller. It is internally synchronized by the VL82C320 before being used to generate HRQ.
DMAHLDA	98	O	DMA Hold Acknowledge - An output sent to the Bus Controller which indicates that the current hold acknowledge is in response to DMAHRQ.
–BRDRAM	99	O	Board DRAM, active low - An output to indicate that on-board DRAM is being addressed.
–EALE	92	O	Early Address Latch Enable, active low - In 286 mode, this signal is generated internally by decode of the CPU status signals. In 386SX mode, the VL82C320's –ADS input is gated directly to the –EALE output.
OUT1	84	I-CMOS	Indicates a refresh request.
PERIPHERAL INTERFACE SIGNALS			
A20GATE	75	I-TTL	Address Bit 20 Enable - An input that is used internally along with Port A bit 1 to determine if A20 is passed through or forced low. It also determines the state of –BLKA20.
TURBO	76	I-TTL	Turbo, active high - This input to the VL82C320 determines the speed at which the system board operates. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET4 and MISCSET3. Turbo mode is active only when all TURBO requests are active.
–RC	77	I-TTL	Reset Control, active low - The falling edge of this signal causes a RESCPU signal.
BUS INTERFACE SIGNALS			
OSC	72	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
–IOR	85	I-TTL	I/O Read, active low - Indicates that an I/O read cycle is occurring on the bus.
–IOW	86	I-TTL	I/O Write, active low - Indicates that an I/O write cycle is occurring on the bus.
RSTDRV	87	I-CMOS	Reset Drive, active high - This signal is used to reset internal logic and to derive RESCPU, and RESNPX.
SDLH/–HL	88	I-TTL	System Data Bus Low-to-High/High-to-Low Swap - This signal is used to establish the direction of byte swaps.
–SDSWAP	89	I-TTL	System Data Bus Byte Swap Enable - This is the qualifying signal needed for SDLH/–HL.
–XDREAD	90	I-TTL	Peripheral Data Bus (XD Bus) Read - This signal determines the direction of the XD bus data flow. When this signal is high, the XD Bus is output enabled.
–LATLO	91	I-TTL	SD Bus Low Byte Latch - This signal is needed to latch the SD bus low byte or XD bus to the local data bus until the end of the bus cycle.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
D15-D0	12-18, 20, 22-29	IO-TTL	CPU Data Bus - This is the data bus directly connected to the CPU. It is also referred to as the local data bus.
SD15-SD0	111-114, 116-119, 122-125, 127-130	IO-TTL	System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from the slot bus.
XD7-XD0	101-107, 109	IO-TTL	Peripheral Data Bus - This bus is connected to the Bus Controller and the VL82C320. It is used to transfer data to/from on-board 8-bit peripherals.
PAR1, PAR0	21, 30	IO-TTL	Parity Bit Bytes 1 and 0 - These bits are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred.
–PARERROR	100	O	Parity Error, active low - This signal is the result of a parity check on all reads from on-board memory.
286/–386SX	78	I-TPU	286 or 386SX Mode - Tied high or left open for 286 mode and grounded for use in 386SX-based systems.
TEST MODE PIN			
–TRI	79	I-TPU	Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are high impedance.
POWER AND GROUND PINS			
VDD	1, 32, 41, 58, 74, 110, 121	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.
VSS	19, 31, 36, 42, 46, 55, 81, 82, 108, 115, 120, 126, 131	GND	Ground connection, 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type	Signal Code	Signal Type
I-TTL	TTL level input	IC-OD	Open drain output
I-TPD	Input with 30k ohm pull-down resistor	O	CMOS or TTL output
I-TPU	Input with 30k ohm pull-up resistor	O-TTL	TTL output
I-TSPU	Schmitt-trigger input with 30k ohm pull-up resistor	O-TS	Three-state output
I-CMOS	CMOS level input	GND	Ground
IO-TTL	TTL level input/ouput	PWR	Power
IT-OD	TTL level input/open drain output		

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATIONS

The sections that follow cover detailed operational information for the various logical groupings of VL82C320 subsystems. In most of these sections, the effect of configurable elements that can be controlled via internal I/O registers is discussed at length. Operation of the indexed I/O registers is repeated in summary form in the "Functional Summary of Indexed Registers" section. However, some lesser configurable functions are described only in that section. Do not assume that the information in that section is discussed elsewhere.

CPU INTERFACE

The VL82C320 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the CPU's bus status and address signals, and decodes the bus access. It then decides whether to handle the bus request itself, or send it off to the VL82C331 ISA Bus Controller.

Local Bus Accesses

The VL82C320 decodes the CPU bus signals and addresses. If the decode points to on-board memory, a bank request is issued to the on-chip DRAM Controller. The DRAM Controller then delivers the appropriate signals to on-board memory and returns a –READYO signal. –READYO may be combined with READY signals from the coprocessor or other external devices on the D bus to form the final –READY signal driven to the CPU.

Slot Bus Accesses

The CPU makes slot bus accesses when the VL82C320 decodes the CPU's control signals as either an I/O cycle, INTA cycle or an off-board memory access (the latter includes ROM accesses). In this case, the VL82C320 latches and decodes the CPU's control signals and sends out bus cycle status signals to the Bus Controller. The Bus Controller handles control of the slot transfer. The CPU is prevented from executing another cycle until the slot cycle is completed. During a slot cycle, the –READY signal returned to the CPU from the VL82C320 is delayed until the Bus Controller notifies the VL82C320 that it has completed the data transfer via –CHREADY.

Other CPU Interface

Bus arbitration is handled with the VL82C320's DMAHRQ, DMAHLDA, OUT1, HRQ, and HLDA signals. When the VL82C320 receives an active DMAHRQ (DMA hold request) from the Bus Controller, it synchronizes the HRQ (hold request) signal with the CPU clock and relays it to the CPU. The CPU responds with HLDA (hold acknowledge) to the VL82C320 which then delivers DMAHLDA to the Bus Controller. When the system memory refresh timer expires, HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

Reset control is supplied by the VL82C320. The VL82C320 contains the PS/2®-compatible Port A. It contains a bit that can be set to cause a CPU reset. A second I/O address is provided to perform the same function. The latter option is supplied for Special Features compatibility. These two controls are combined with RC (reset control) input and a RSTDRV (reset drive) hard reset to produce the synchronized RESCPU (CPU reset) delivered to the CPU. (Refer to the section "System Reset Options" for details.)

Coprocessor interface is also supplied by the VL82C320. If the system contains a coprocessor, the interface signals (–ERRORNPX, –BUSYNPX, and PEREQNPX) are sent from the coprocessor to the VL82C320 and decoded to produce the proper interface signals for the CPU. The same decode determines activation of the RESNPX output to the coprocessor. This interface provides PC/AT-compatibility for use with the 287 or 387SX.

BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION CHANNEL

The asynchronous interface to the Bus Controller is handled by a group of signals from the VL82C320. –CHS0, –CHS1, and CHM/–IO define which type of cycle is to be executed as in the table below.

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

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ISA Bus Clock Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	SD Drive	Slow CLK2 Divider	**Bus Clock Divider**	**Bus Mode**

The VL82C286 chip set is capable of supporting AT slot bus operation asynchronous with respect to the CPU clock. Though the ISA Bus Controller actually drives the slot bus, the VL82C320 is programmed for the specified mode and sources the required clock to the ISA Bus Controller. Whether in synchronous or asynchronous modes, the VL82C320 synchronizes the command interface between itself and the ISA Bus Controller to BUSCLK.

BUSCLK is the AT bus clock provided to the ISA Bus Controller by the VL82C320. It runs at twice the final AT slot bus frequency. MISCSET, shown above, is one of the indexed configuration registers. The lower three bits control sourcing of BUSCLK to the ISA Bus Controller. Bit 0 sets synchronous or asynchronous mode. When set to 1, asynchronous mode is selected and the BUSOSC input is routed to the programmable divider. When set to 0, TCLK2 is output to the driver. Bits 1 and 2 of MISCSET provide for a programmable BUSCLK divider. Values of bits 1 and 2 provide for division from one to four. The programmable BUSCLK divider must be set to provide a BUSCLK of 2X the desired bus frequency. When a 16 MHz external oscillator is used, a ÷1 results in 8 MHz bus operation. Power-on reset defaults to ÷4, synchronous mode. See the section "Functional Summary of Indexed Registers" for more details.

Further programmability of bus timing is afforded by the ISA Bus Controller.

DRAM SUBSYSTEM DESCRIPTION

The VL82C320 supports up to 32 Mbyte of DRAM on the system board in four 16-bit banks. Each byte contains its own parity bit for a total of 18 bits per bank. A single bank can consist of 256K, 1M, or 4M DRAMs.

The parts used in multiple banks can consist of all one DRAM type or mixtures of any two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported.

The VL82C320 supports four banks by providing four –RASBK signals and eight –CAS signals. This allows direct drive with no external buffering.

Several configuration registers internal to the VL82C320 are used to control the memory map, interleaving, DRAM timing, and page mode. These features are discussed in the following sections. Since interleaving requires pairs of banks, various controls described next act on memory in bank pairs. The short hand notation Bank A is used when describing something that affects DRAM banks 0 and 1 as a set. Similarly, Bank B is used to describe DRAM banks 2 and 3 as a set.

Memory Maps

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (03)	ROMSLOT	1	1	**DRAM Memory Map Code**				

The VL82C320 supports 26 memory maps. These maps are shown in Table 1. The table shows the DRAM combinations that are addressable in each of four 16-bit memory banks. The memory column shows the total system memory available in each memory map. The RAMMAP4-RAMMAP0 column indicates the hex value written in bits 4-0 of the RAMMAP indexed configuration register in order to select each map. It should be noted that banks 0 through 3 in Table 1 refer to the "logical" banks as internally addressed by the VL82C320. The actual system board memory banks accessed by the internal signals may differ depending on the value stored in indexed configuration register RAMMOV. See the section "DRAM Remap Options" for more details.

TABLE 1. DRAM MEMORY MAPS SUPPORTED

Bank 0	Bank 1	Bank 2	Bank 3	Memory MB	RAMMAP (4-0)
256K				0.5	0
256K	256K			(1.38)1.0	(1F*)1
256K	256K	256K		1.5	2
256K	256K	256K	256K	2.0	3
1M				(2.38) 2.0	(1E*) 4
256K	1M			2.5	5
256K	256K	1M		3.0	6
1M	1M			4.0	7
1M	1M	256K		4.5	8
256K	256K	1M	1M	5.0	9
1M	1M	1M		6.0	A
1M	1M	1M	1M	8.0	B
4M				8.0	C
256K	4M			8.5	D
256K	256K	4M		9.0	E
1M	4M			10.0	F
1M	1M	4M		12.0	10
4M	4M			16.0	11
4M	4M	256K		16.5	12
256K	256K	4M	4M	17.0	13
4M	4M	1M		18.0	14
1M	1M	4M	4M	20.0	15
4M	4M	4M		24.0	16
4M	4M	4M	4M	32.0	17

*1Fh and 1Eh are special cases where the 384K of memory above 640K is mapped as extended memory. EMS and shadow RAM are unavailable in these two modes. Memory map 1h allows EMS and shadowing, but no extended memory. Memory map 0h is the only case where there is no DRAM available for shadow, extended, or expanded memory. Memory maps other than these four can support shadow, extended, and expanded memory.

DRAM Remap Options

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMOV (04)	1	1	1	1	RAS - CAS Swap Code			

The RAMMAP register described in the previous section shows 26 distinct memory maps that are available in a TOPCAT based system. Those are actually logical memory maps. The addition of the RAMMOV function provides 16 different ways to map the logical maps into the four possible physical DRAM banks. The combination of these two register functions provides a large number of unique ways to create a valid TOPCAT memory map. This capability provides two key features for the end user.

Easier DRAM Memory Upgrades

The physical DRAM banks need not be populated in the same order as would normally be dictated by the RAMMAP options alone. One example of when this is useful is the case where a system with one bank of 1M DRAMs is upgraded by adding a second bank of 256K DRAMs. Without the RAMMOV feature, it would be necessary to remove the 1M DRAM bank and move it to physical bank 1 then put the 256K DRAMs in physical bank 0. Using RAMMOV allows the 1M DRAMs to be left in place. The 256K DRAMs may be placed in any of the three available physical DRAM banks remaining. The proper RAMMOV code is then programmed so that the logical memory map (RAMMAP = 5h) is correctly routed to the proper physical DRAM devices.

DRAM Error Recovery

In case of a partial or total DRAM bank failure, the remaining functional DRAMs can be switched into an alternate, valid logical memory map by reprogramming RAMMOV and RAMMAP together.

Table 2 shows the 16 logical to physical mappings that are available. In the top row of this chart, the numbers 3, 2, 1, and 0 directly under "DRAM Bank Mapping" refer to the four physical DRAM memory banks. In the 16 rows beneath, the code that must be programmed into the RAMMOV register bits 4-0 is shown on the left side of the chart. On the right side is shown the logical bank that is mapped to the corresponding physical bank shown in the top row.

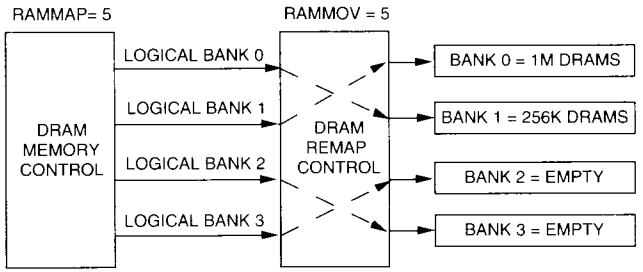
As an example, consider RAMMOV code 0001b shown in Table 2. Accesses to logical bank 3 are directed to physical bank 3. Accesses to logical bank 0 are directed to physical bank 2. Accesses to logical bank 2 are directed to physical bank 1. Accesses to logical bank 1 are directed to physical bank 0.

Note that when RAMMOV = 0000b, the default condition, the logical banks are directed to the same physical bank numbers.

TABLE 2. REMAP CONFIGURATION REGISTER CODE

RAMMOV Code				DRAM Bank Mapping				
D3	D2	D1	D0	3	2	1	0	Physical DRAM Banks
0	0	0	0	3	2	1	0	
0	0	0	1	3	0	2	1	
0	0	1	0	3	1	2	0	
0	0	1	1	3	0	1	2	
0	1	0	0	3	1	0	2	
0	1	0	1	2	3	0	1	
0	1	1	0	2	1	0	3	
0	1	1	1	2	0	1	3	Logical DRAM Banks
1	0	0	0	1	3	2	0	
1	0	0	1	1	2	3	0	
1	0	1	0	1	0	2	3	
1	0	1	1	0	3	2	1	
1	1	0	0	0	2	3	1	
1	1	0	1	0	2	1	3	
1	1	1	0	0	1	3	2	
1	1	1	1	0	1	2	3	

Example: Upgrading from one 1M DRAM bank to one 1M and one.256K bank.



Page Mode/Interleave Subsystem Overview

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05)	DRAM Drive		ESTART	1	Page Mode A	Page Mode B	Bank A Int	Bank B Int

In order to raise performance and decrease system cost, both page mode and interleave operation are available on the system board DRAM. Interleave options are selected by the programming of the RAMSET and RAMMAP configuration registers. Page mode is enabled or disabled for each pair of DRAM banks independently. When on, it is active on all memory maps for the enabled bank pairs. Interleaving requires pairs of banks. Detailed operation of each is given in the following sections.

Interleave Operation

Two-way interleaving is automatically enabled whenever both banks of a pair are populated with like DRAM types. If all four banks are populated with like DRAMs, four-way interleaving automatically occurs when both bank pairs are programmed to interleave on the same bit. If not, two-way interleaving occurs. If the four banks are not populated with like DRAMs, two-way interleaving occurs on pairs that are of the same type. In a machine with three banks populated, the first two banks two-way interleave if they are of the same type. The third does not interleave. Table 3 shows the automatic interleaving options that occur versus the number of populated banks. All combinations not shown are unsupported. Table 3 also shows that 0, 1, 2, and 3 are the designations for each of the four DRAM banks. In the columns below these designators, "Yes" or "No", indicate whether the bank is populated. There is no configuration register programmability for enabling the interleave mode. All interleaving options (none, two-way, or four-way) occur automatically as the result of the memory map programmed into RAMMAP.

While the use of interleave is automatic and not programmable via the configuration registers, it is possible to select which bit is used for interleaving. Configuration register RAMSET bit 1 programs the Bank A interleave and bit 0 programs the Bank B interleave. When set to 0, interleave occurs on bit 1. This is called "word interleaving". When set to 1, interleave occurs on bit 10 regardless of DRAM types used. This is called "block interleaving". When all four DRAM banks are populated with like part types and bit 0 and bit 1 are set differently, two-way interleaving occurs. When they are the same, four-way interleaving occurs.

Page Mode Operation

Interleaving operates independently of page mode. Once the desired interleave bits are set, the remaining interleave modes are automatically selected by the programmed memory map. Page mode control is given by two configuration register bits in the RAMSET register. Bit 3 = 1 enables page mode operation on DRAM banks 0 and 1. Bit 2 = 1 enables page mode operation on banks 2 and 3.

When activated for a bank pair, page mode is active whether one bank or both are populated. When four-way interleaving is active it is possible to have page mode active on either, neither, or both DRAM bank pairs. This does not impact the automatic interleaving, though it impacts performance.

When pairs of banks are installed interleaving is automatically enabled. The combination of page mode with interleaving results in the best possible combination of fast system memory operation using the most cost-effective DRAMs. When accesses interleaved between banks occur, CAS precharging of the next bank to be accessed occurs while CAS is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page hit cycles.

Tables 4, 5, and 6 show how the CPU address lines are used to accomplish the interleave options possible with the three supported DRAM types. The top portion of each table shows the CPU address lines that are strobed onto MA0-MA10 by CAS, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA0-MA10 by –RASBK, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

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TABLE 3. AUTOMATIC INTERLEAVE VS. MEMORY MAP

Bank 0	Bank 1	A Bank Address Mode	Bank 2	Bank 3	B Bank Address Mode
Yes	No	Linear	No	No	N/A
Yes	Yes	2-Way Interleave	No	No	N/A
Yes	Yes	2-Way Interleave	Yes	No	Linear
Yes	Yes	2-Way Interleave 0 and 1*	Yes	Yes	2-Way Interleave 2 and 3*

* This is for the case where Banks A and B contain different types of DRAMs. For memory maps 03h, 0Bh, and 17h, all four banks contain the same DRAM type and four-way interleaving is used if both bank pairs interleave on the same bit.

TABLE 4. 256K DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	13	13	5
	12	12	12	12	12	6
	11	11	11	20	20	7
	10	19	19	19	19	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	19					
	20	20	20	–	–	
	21	21	21	21	21	
	22	22	22	22	22	
	23	23	23	23	23	
	24*	24*	24*	24*	24*	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Note: For the 256K options: CA10 = A12 for RAMMAP = 13; A11 for all others.
CA9 = A11 for RAMMAP = 9, 13; A10 for all others.
RA10 = A22 for RAMMAP = D, E; A23 for all others.
RA9 = A20 for RAMMAP = 5, 6; A21 for all others.

TABLE 5. 1M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	10	11	11	12	12	9
	–	–	–	–	–	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	13	13	5
	12	12	12	22	22	6
	11	20	20	20	20	7
	19	19	19	19	19	8
	20	21	21	21	21	9
	–	–	–	–	–	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	21	–	–	–	–	
	22	22	22	–	–	
	23	23	23	23	23	
	24*	24*	24*	24*	24*	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Note: For 1 Megabyte options: CA10 = A12 for RAMMAP = 15; A11 for all others.
RA10 = A22 for RAMMAP = F, 10; A23 for all others.

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TABLE 6. 4M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	10	11	11	12	12	9
	11	12	12	13	13	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	24*	24*	5
	12	22	22	22	22	6
	20	20	20	20	20	7
	19	19	19	19	19	8
	21	21	21	21	21	9
	22	23	23	23	23	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	23	24*	24*	–	–	
	24*	–	–	–	–	
	–	–	–	–	–	
	–	–	–	–	–	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Programmable Memory Timing

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RASTMA (07)	RAS ADDSEL	tRCD	1	tRP		tRAS		
CASTMA (08)	tCASW		tCST	tCP		1	tCASR	
RASTMB (09)	RAS ADDSEL	tRCD	1	tRP		tRAS		
CASTMB (0A)	tCASW		tCST	tCP		1	tCASR	

System board memory timing for this chip set is not specified in wait states. Instead, each of the critical DRAM timing parameters is specified as a number of programmable clock cycles. This allows virtually unlimited flexibility in matching DRAM specs to system CPU speed. The number of wait states for the system is whatever falls out of the programmed parameters. Banks A and B are programmed separately. This allows a user who later adds memory to maximize the speed advantage of faster parts when these chips are accessed. Conversely, a user can add slower parts for a cost savings without slowing down accesses to the entire memory system.

Four configurations registers are used to program the DRAM timing parameters. RASTMA allows programming of RAS ADDSEL delay, tRCD, tRP, and tRAS parameters for banks 0 and 1. RASTMB performs the same functions for banks 2 and 3.

CASTMA allows programming of tCST, tCP, tCASR, and tCASW for banks 0 and 1. CASTMB performs the same functions for banks 2 and 3.

The section "Functional Summary of Indexed Registers" discusses the range programmability for each parameter. Figures 2 and 3 show the relationship between these programmable timing signals for page and non-page mode operation.

FIGURE 2. –RASBK/–CAS TIMING MODEL

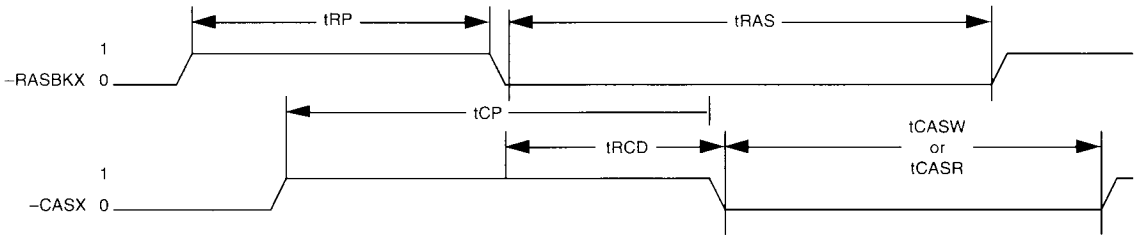
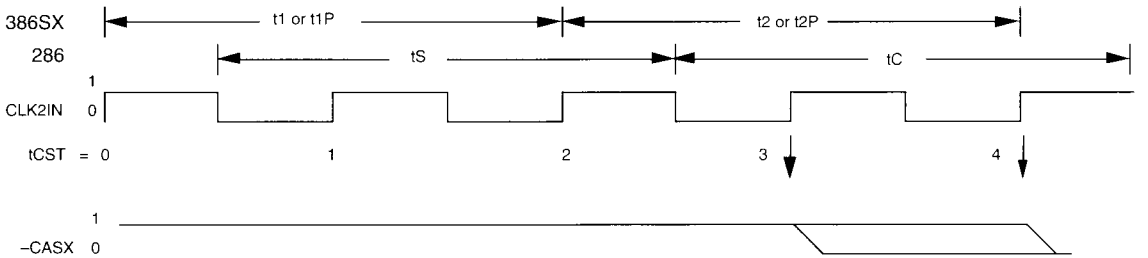
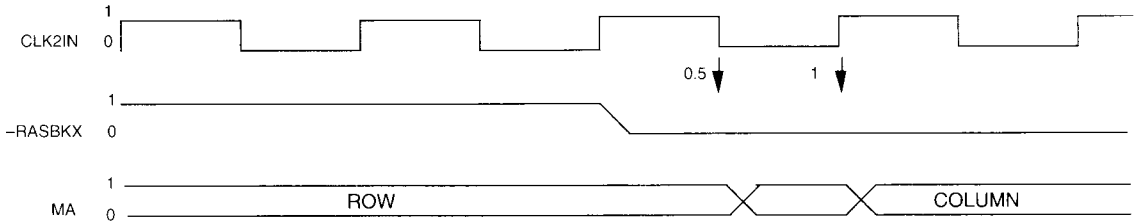


FIGURE 3. –CAS START TIME (tCST) TIMING MODEL



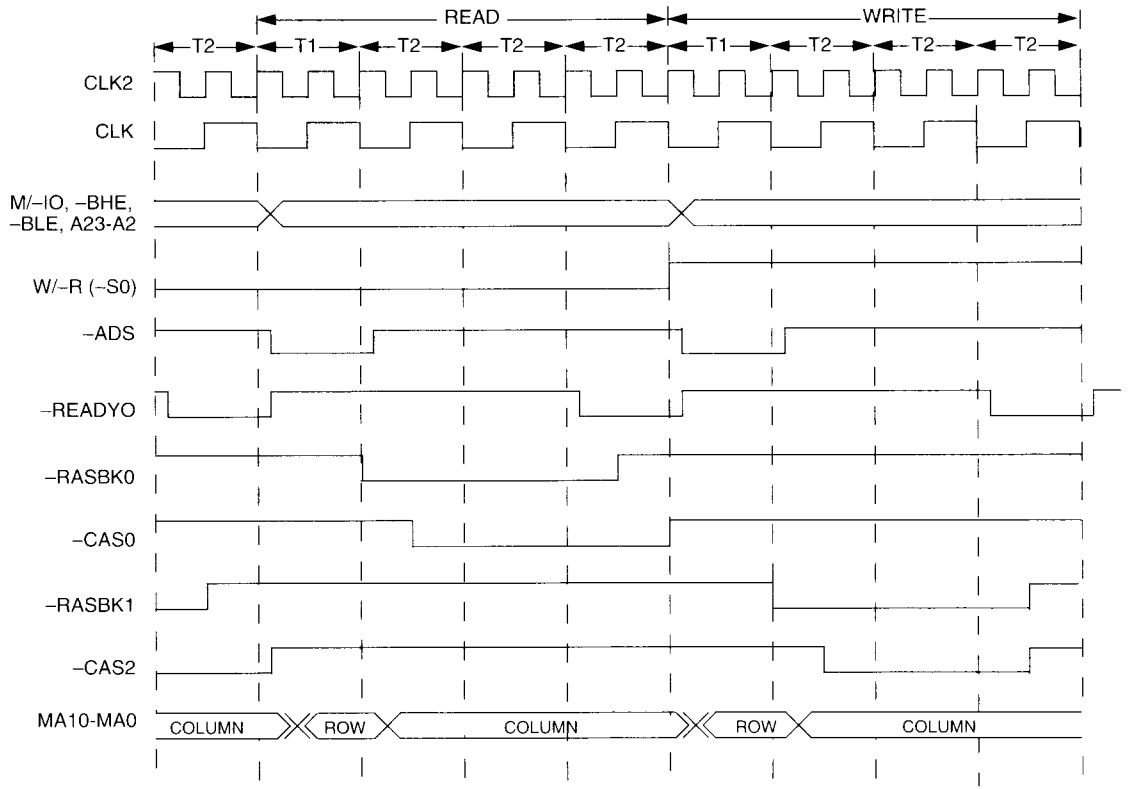
Note: tCST applies to write cycles only and equals 3 or 4. During read cycles, CAS start time defaults to zero CLK2's for pipelined or two CLK2's for non-pipelined SX or 286 mode. If ESTART bit in RAMSET register is programmed inactive (1), then add one to start times just mentioned for reads only. This is the earliest time –CAS can start for read cycles. Actual –CAS start time may be delayed due to –CAS pre-charge or –RASBK to –CAS delay time not yet met.

FIGURE 4. –RAS TO ADDSEL TIMING MODEL



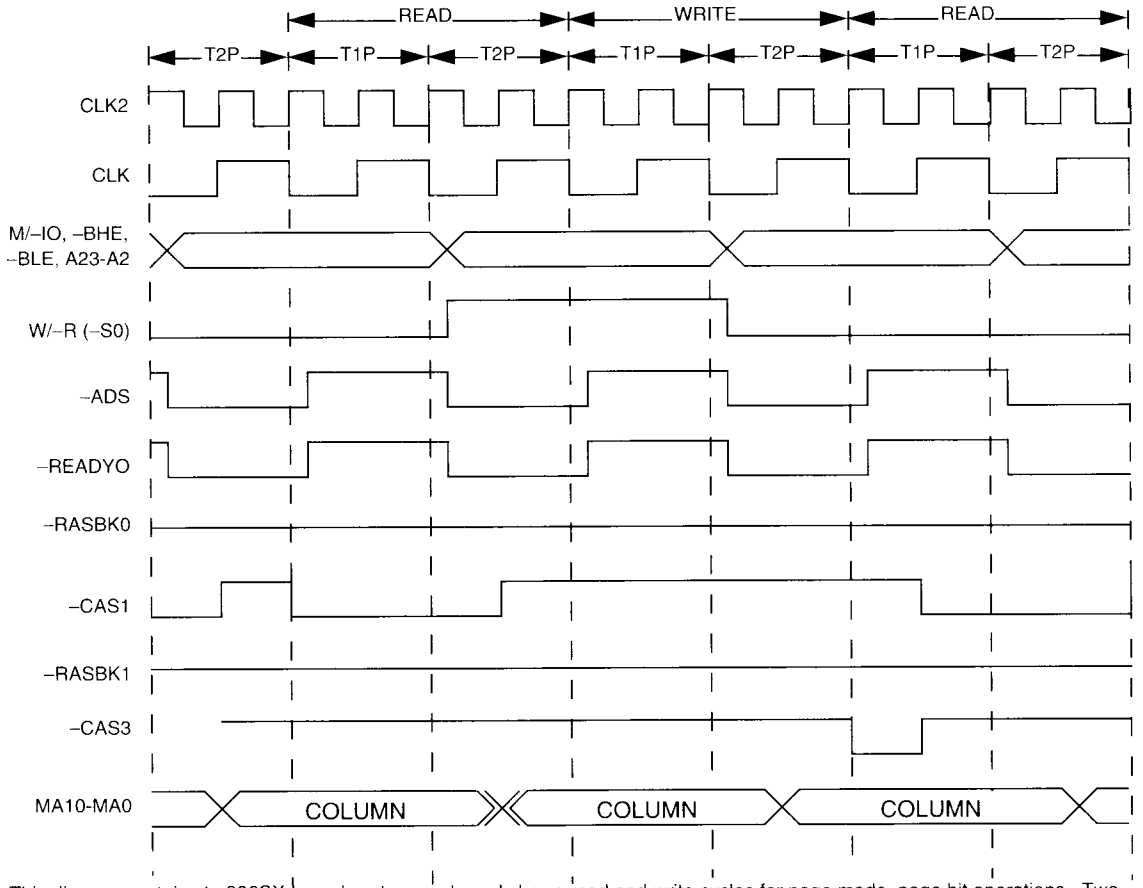
Note: Address Select can be programmed to switch MA lines 1/2 CLK2 or one CLK2 cycle after –RASBK.

FIGURE 5. NON-PAGE MODE, TWO-WAY INTERLEAVE, NON-PIPELINED



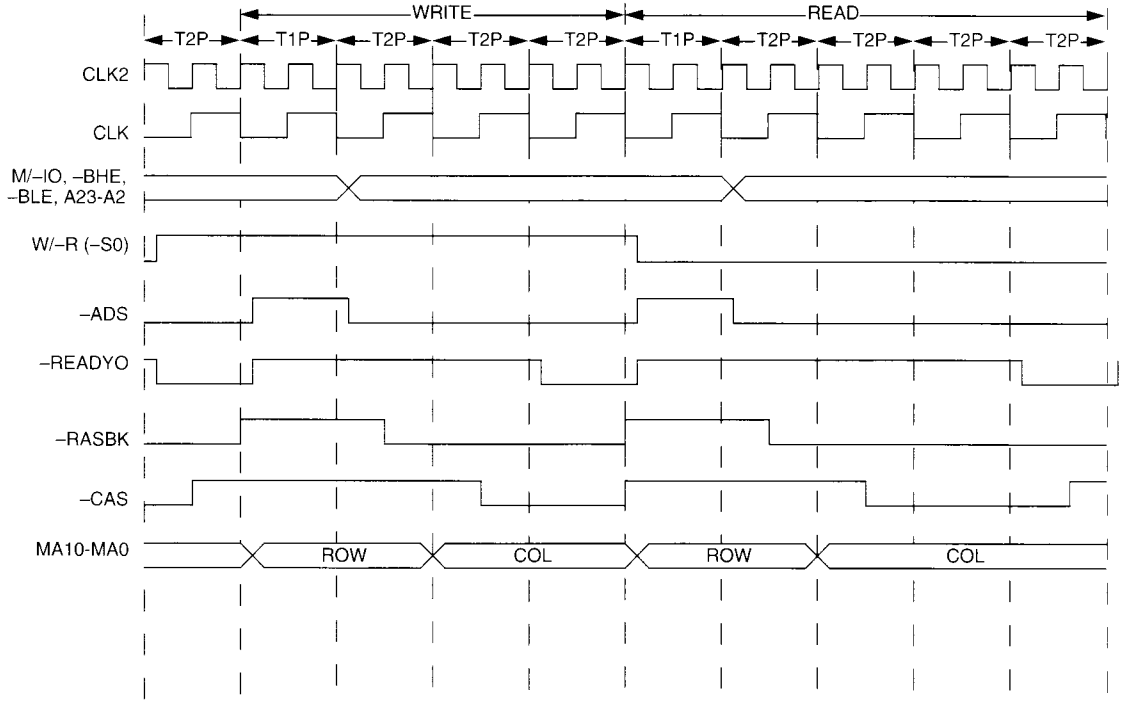
This diagram pertains to 386SX-based systems only and shows a read and write cycle with on-board memory on the D bus. Signals shown are for a two-way interleaved cycle to the first two banks (low byte) of system memory in non-pipelined mode. The –RASBK, –CAS, and MA signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is active (0).

FIGURE 6. PAGE MODE, PAGE HITS, PIPELINED, TWO-WAY INTERLEAVED



This diagram pertains to 386SX-based systems only and shows read and write cycles for page mode, page hit operations. Two-way interleaving is shown on the first two memory banks for a pipelined cycle. The –RASBK and –CAS signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is programmed active (0).

FIGURE 7. PAGE MODE ON (PAGE MISSES)



This diagram pertains to 386SX-based systems only and shows a read and write cycle for page mode, page miss operations. The –RASBK and –CAS signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is programmed active (0).

Programmable Refresh Control

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06)	0*	RESERVED			10/16 IO	Refresh Divider		

*Alway write a 0 to bit D7.

Power-up Defaults

The DRAM system resets to a default state on power-up that allows any configuration to run, although it is a less than optimum state until BIOS or POST configures the registers with desired values. The defaults are:

- One bank of 256K DRAM
- Direct mapping from logical to physical DRAM banks
- Page mode on
- Timing for 120 ns DRAMs in 25 MHz systems

Hold Request Arbiter

The hold request arbiter is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 in the Bus Controller issues a hold request via the DMAHRQ signal or when the output of Counter 1 in the 8254 megacell of the Bus Controller makes a low-to-high transition. This latter signal is the OUT1 signal from the Bus Controller to the VL82C320.

At the end of a hold request from either source, the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the HRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the HRQ signal and return control back to the CPU. The acknowledge to the DMA is via the VL82C320's DMAHLDA output. For refresh cycles, an acknowledge occurs in the form of an active signal on the VL82C320's –REFRESH pin.

System Board DRAM Refresh

The VL82C320 performs on-board DRAM refresh and controls both on- and off-board refresh timing.

The VL82C320 refresh circuitry controls system board refresh and slot bus refresh in a synchronous manner. The division specified by bits 2-0 applies to on- and off-board refresh.

If bits 2-0 of the REFCTL register are set to their default value of 0h, the 15 µs, compatible timing is used. Other valid values, as specified in the section "Functional Summary of Indexed Registers," cause the refresh to occur at a slower rate in support of newer, low power, slow refresh DRAMs. These slower rates are all divisions of the normal 15 µs timer provided by the Bus Controller on pin OUT1.

In sleep mode, –CAS before –RAS refresh may be used for on-board memory. This significantly reduces power requirements. The DRAMs generate their own refresh addresses internally. Therefore, the VL82C320 is not required to drive the memory address bus during refresh. When not in sleep mode, –RAS only refresh mode is used.

4

SLTPTR - Critical Memory Control Element

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLTPTR (02)	A23	A22	A21	A20	A19	A18	A17	A16

SLTPTR is a pointer to a 64K memory boundary between 256K and 16M. Eight bits are required to specify this range. They are used to compare to address lines A16-A23. SLTPTR sets the 64K boundary above which CPU addresses are directed to the AT slot bus. Any system board memory from 1 Mbyte up to SLTPTR is accessible as on-board extended memory. From SLTPTR up to 16 Mbytes, slot bus DRAM extended memory resides.

When the on-board EMS backfill system is disabled, SLTPTR can also be set below 1 Mbyte. At least one bank of 256K RAMs must be on the system board on reset for a physical memory size of 512K. The minimum valid value for SLTPTR is 04h to allow slot memory cards, especially EEMS capable boards, to backfill down to 256K. This capability is provided for any users who prefer to not use the built-in EEMS system. Any value between 04h and 09h makes the portion of system board DRAM from that address to A0000h inaccessible when the on-board EMS system is inactive. The set of usable values for SLTPTR is 04h to FDh. A value of FEh or FFh results in no off-board accesses since CPU accesses in the FE0000h and FF0000h segments always result in ROM chip selects. Any out of range value is treated the same as FFh.

Exceptions to the above are SLTPTR values 000Ah through 000Fh whose access is determined by the configuration of indexed registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS described in the "EMS Subsystem" sections. Therefore, setting SLTPTR between 0Ah and 0Fh is treated the same as if the value were 10h. Default = FFh. Also see the description of the additional memory control feature provided by CTRL1 bits 7-6.

Note: The slot pointer must point to 1M or higher (≥10h) if use of the EMS backfill registers is required. Pointing SLTPTR below 640K and using the backfill registers is incompatible. Therefore, any time the SLTPTR is set between 00h and 09h the EMS backfill register enable bit in configuration register EMSEN1 is cleared. A smart BIOS setup routine does not allow this condition in actual operation.

EMS Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
EMSEN1 (0B)	EMS Enable	BF Enable	Reserved	EMS MAP	B/EC000	BE/8000	B/E4000	B/E0000
EMSEN2 (0C)	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000

The EMS system consists of 72 mapping registers. They are split into a standard and alternate set of 36 registers each. The VL82C286 chip set supports the full LIM EMS 4.0 specification with any of the valid memory maps of 1 Mbyte and higher. The alternate register set allows rapid hardware context switching. Note that the VL82C286 chip set is capable of translating addresses via the EMS registers over the entire 32 Mbyte range of possible system board memory.

The EMS system is split into two parts, the 12 EMS page registers which cover the range from C0000h to EFFFFh and the 24 backfill registers that cover 40000h to 9FFFFh. Bit D7 of configuration register EMSEN1 is a global enable for the EMS page registers. Each of the 12 registers can then be individually disabled if there are system address conflicts. Bits 0 through 7 of EMSEN2 and bits 0 through 3 of EMSEN1 provide this function. The 24 EMS backfill registers are enabled by setting bit 6 of EMSEN1. These registers are all enabled or all disabled. No individual control is provided. If a full LIM EMS 4.0 system is desired, both bits 6 and 7 of EMSEN1 are set as are the desired EMS page register enable bits. Note that when EMS enable, bit 7 = 0, the state of BF enable, bit 6, has no effect on the system.

The normal EMS page register mapping to C0000h-EFFFFh can be altered by changing EMSEN1 bit 4 from 0 to 1. In this case, the 12 page registers map to AXXXXh, DXXXXh, and BXXXXh in that order. In this case, EMSEN1 bits 3-0 work to enable or disable the BXXXXh registers rather than the EXXXXh registers. Similarly, EMSEN2 bits 3-0 work to enable or disable the AXXXXh registers rather than the CXXXXh registers.

When the backfill EMS registers are not used, the EMS driver allocates all memory above SLTPTR for EMS page memory. It also can use the system board memory at the same addresses as the enabled EMS page registers and any other 16K segments in the A0000h to BC000h and F0000h to FC000h areas for which the shadow code is 00b as set in configuration registers AAXS, BAXS, and FAXS. When the backfill registers are active, EMS pages can also be allocated for all system board memory from 40000h to 9FFFFh. There is no wasted DRAM in a VL82C286-based system. All memory not allocated for other purposes can be used as expanded memory.

The SLTPTR has critical effects on the EMS system. Only one effect is hardware related. When SLTPTR is set to a value from 0004h to 0009h, bit 6 of EMSEN1 is cleared. This disables the EMS backfill registers. Placement of SLTPTR is otherwise used by the EMS driver to determine the area of memory that can be allocated for use as EMS pages. Table 7 summarizes the effect of SLTPTR on the EMS system.

The EMS driver also interacts with the shadow control system through configuration registers AAXS through FAXS. Any enabled EMS page registers override the shadow control in their respective 16 Kbyte ranges. System board memory at the same address range as the EMS page registers can be allocated to the EMS memory pool by the EMS driver software. In addition, other non-EMS 16K segments can be allocated to the pool if they are not shadowed or otherwise in use. This is determined by the two shadow control bits for a specific segment. When the bits are 00b, the system board memory may be allocated to the pool. Table 8 summarizes the interaction between EMS and shadow control.

TABLE 7. SLTPTR WITH EMS SYSTEM ENABLED

Slot Pointer Location	Effect
256K-640K	EMS backfill register automatically disabled. EMS page registers remain operational.
	CPU addresses 0 to SLTPTR are on-board DOS memory accesses.
	CPU addresses SLTPTR to 16M are slot memory accesses.
	On-board memory > SLTPTR = EMS /Shadow memory.
640K-1M 000Ah-000Fh	Respond as if SLTPTR = 0010h. (See next case.)
1M-16M 0010h-0100h	CPU addresses 0 to 640K is system board DOS memory if backfill is not enabled, otherwise, CPU addresses 0 to 256K is system board memory.
	CPU addresses 1M to SLTPTR are system board extended memory accesses.
	CPU addresses from SLTPTR to 16M accesses slot bus extended memory.
	EMS translation accesses system board RAM from SLTPTR to RAM top. Also system board RAM from 256K to 640K if backfill EMS is enabled.

Note: Table 7 does not mention what occurs for accesses between A0000h and FFFFFh. When EMS is off, the result of CPU accesses to this memory region is determined solely by configuration of registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. When the EMS system is enabled, the active EMS registers between CXXXXh and EXXXXh override the settings in any areas that overlap the configurations in CAXS, DAXS, and EAXS. CPU addresses that fall in the realm of EMS register control are not directly passed to the slots or the system board. The addresses are translated and access reserved areas of system board DRAM above SLTPTR or unused areas below 1 Mbyte. Table 8 summarizes the rules that are followed for all cases.

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TABLE 8. INTERACTION BETWEEN EMS AND SHADOW CONTROL

EMS Enable (Bit 7)	EMS Page Enable	Shadow Control		Effect
0	Don't Care	0	0	R/W slot bus or ROM chip selects.
		1	0	Read system board or write slot (shadow).
		1	1	R/W system board.
		0	1	Read slot or ROM chip selects, write system board.
1	0 (Note 1)	0	0	CPU accesses slots, EMS may access on-board DRAM.
		1	0	Shadowed, EMS does not use.
		1	1	Used by other resource, EMS driver does not allocate.
		0	1	Setup mode active. EMS driver does not allocate (Note 2).
1	1 (Note 3)	X	X	EMS overrides use of this area.
				CPU accesses translated by EMS. System board DRAM used by EMS system for EMS memory pages.

Note 1: This case not only applies to the areas from C0000h to EFFFFh for which the EMS enable bit is turned off, but also to the A0000h to BFFFFh and F0000h to FFFFFh areas of memory. This information is supplied for use by the EMS driver code developers. Hardware operation in this mode is the same as the first case listed in Table 7.

Note 2: When an EMS driver is installed, this case should not exist. A shadow setup routine uses this code. It then changes it to 10b to enable the shadow feature. However, if an EMS driver sees this code, it may allocate the system board DRAM in this area.

Note 3: In the areas where active EMS registers reside in the CXXXXh to EXXXXh area, the control bits are overridden. Any CPU accesses to this memory space are translated and the system board memory at these addresses is allocated to the EMS page memory pool.

TABLE 9. EMS INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
	Set #	Auto-inc	A5	A4	A3	A2	A1	A0
	0 = Std 1 = Alt	0 = Off 1 = On						

Data Port	Page Segment	Data Port EBh								Data Port EAh							
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	C0/A0	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	C4/A4	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
2	C8/A8	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
3	CC/AC	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
4	D0000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
5	D4000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
6	D8000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
7	DC000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
8	E0/B0	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
9	E4/B4	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
A	E8/B8	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
B	EC/BC	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
C	40000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
D	44000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
E	48000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
F	4C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
10	50000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
11	54000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
12	58000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
13	5C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
14	60000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
15	64000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
16	68000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
17	6C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
18	70000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
19	74000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1A	78000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1B	7C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1C	80000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1D	84000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1E	88000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1F	8C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
20	90000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
21	94000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
22	98000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
23	9C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14

Note: A 1 indicates reserved bits that read back as logic 1.

Table 9 shows a programmer's model of the register set. Registers 0h to Bh are called the EMS page registers. Registers Ch to 23h are the backfill registers. The register set is accessed by writing a command byte to the index register located at I/O address E8h. Bits D0-D5 contain the address of the desired EMS register from 0 to 35. Setting bit D6 to a 1 activates auto-increment. This feature is described in detail below. Bit D7 contains the desired register set to be accessed; the standard or the alternate set. I/O port addresses EAh and EBh then provide a window into the page register specified in the index register. Address EAh allows access to A14-A21. EBh allows access to A22-A24. Sixteen-bit I/O reads and writes can be used to gain access to A14-A24 in one operation via address EAh.

After initial accesses to port addresses at EAh and EBh, subsequent accesses are to the same page segment register until a new register number is written to the lower six bits of the index port at port address E8h or unless bit D6 of the index port was previously set to a logic 1. In this case, any access to port address EBh increments the page register number. (This new value is seen by a read to the index register port E8h.) The next read or write is to the next sequential page register. This feature allows the entire register set to be changed with a single access to the index register with either byte or word I/O access. For byte accesses, the lower byte at port address EAh must be written first. The access to the upper byte at EBh causes an auto-increment. Since all word accesses are made to port EAh, each one causes an auto-increment. This is due to the fact that the chip set actually breaks the word into two byte chunks, writing EAh followed by EBh.

The auto-increment feature speeds the already fast hardware driven context switching capability by minimizing the number of software instructions and, therefore, machine cycles required to read and save one context of the EMS registers, then retrieve and write another.

Configuration Enable/Disable

A write to port F9h with MISCSET7 = 0 causes EMS ports E9h, EAh, and EBh to become read-only until a write to port FBh occurs. E8h remains read/write. This allows the EMS Data Registers to be read but not modified. More information on this feature is available in the "Dedicated Internal Control Registers" section.

Shadow RAM Subsystem

Data Port EDh (R/W)	D7 D6	D5 D4	D3 D2	D1 D0
AAXS	AC000 Access	A8000 Access	A4000 Access	A0000 Access
BAXS	BC000 Access	B8000 Access	B4000 Access	B0000 Access
CAXS	CC000 Access	C8000 Access	C4000 Access	C0000 Access
DAXS	DC000 Access	D8000 Access	D4000 Access	D0000 Access
EAXS	EC000 Access	E8000 Access	E4000 Access	E0000 Access
FAXS	FC000 Access	F8000 Access	F4000 Access	F0000 Access

Six indexed configuration registers are provided to give complete control over each of the 64K memory segments between 640K and 1M. The registers are called AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. Each register contains two bits for each 16K paragraph in the 64K segment controlled by that register. Refer to the section "Functional Summary of Indexed Registers" for more details.

The four modes provided are:

1. Normal PC/AT-compatible operation. This is R/W slot bus or ROM chip select depending on the memory space.
2. R/W system board DRAM. This allows complete access to DRAM in the given 16 Kbyte region.
3. Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for mode 2. In this mode, writes are directed to the slot bus.
4. Shadow setup mode. In the E000 and F000 segments, reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments A000 to D000 reads are from the slot bus and writes are to the system board DRAM. This allows shadowing of system board ROM as well as ROMs on a slot card.
5. Shadow RAM areas are only accessible from the CPU, not from DMAC or Masters.

NUMERICAL PROCESSOR INTERFACE

The VL82C320 supports either the 287 or 387SX numeric coprocessors (NPX) for use in high performance floating point math applications. In a 286-based system, only the 287 may be used. Similarly, a 386SX-based system requires a 387SX coprocessor. It is not possible to mix CPUs and coprocessors.

The VL82C320 contains several dedicated pins in order to provide the interface between the NPX and CPU. The following sections describe the interface logic broken into several parts.

System Reset Logic

System reset is an internally generated signal caused by a reset signal to the VL82C320 (RSTDRV), usually in response to the POWERGOOD signal. This signal initiates a reset to the CPU and to the NPX.

CPU-only Reset Logic

A CPU reset without a coprocessor reset can occur for one of two reasons. The first is usually done in order to switch from protected to real mode. The signal which causes it is shown as "Hot" reset. It is triggered by setting bit 0 of I/O port 92h to a 1, by a read of I/O port EFh, or by receipt of an external –RC signal. The latter signal causes a CPU-only reset as soon as received. There is a 6.72 µs delay between the occurrence of either of the first two events and activation of the RESCPU signal.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset.

In both of the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

NPX-only Reset Logic

For PC/AT compatibility, NPX-only reset is provided via a I/O write to F1h. This action provides a reset to the NPX synchronized to CLK2 of 80 CLK2 cycles duration. –READYO does not go active after the write to F1h for 80 CLK2 cycles after the falling edge of RESNPX. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387SX into the same internal state as does a reset of the 287. For this reason, the F1h reset function may be disabled by setting configuration register MISCSET6 = 1.

Error/Interrupt Logic

For PC/AT-compatibility, –ERRORNPX active generates interrupt 13. It also latches –BUSYCPU active. This later action is required in order to prevent the CPU from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler clears the latched –BUSYCPU by performing a write to I/O port F0h.

Busy Logic

The –BUSYCPU signal can be produced from three sources. It always occurs in response to the –BUSYNPX input. It also occurs as latched by the –ERRORNPX signal as previously described. Busy test logic is invoked only on system reset. At this time, the 386SX self-test mode is triggered. This adds 33 ms at 16 MHz and 21 ms at 25 MHz to the CPU reset time. At the end of the self-test the BIOS can read the CPU self-test result register and perform whatever function is desired on failure. Note that when a CPU-only reset is invoked, this self-test is not performed. Therefore, "Hot" resets are performed as fast as possible.

PEREQ Logic

The PEREQNPX signal is always passed directly to the PEREQCPU pin. In addition, PEREQCPU is driven and held active as soon as –BUSYNPX goes inactive after occurrence of an active –ERRORNPX signal. The PEREQCPU signal returns to following the PEREQNPX signal after a write to I/O port F0h is performed by the NPX interrupt 13 service routine. In 286-based systems the PEREQCPU/PEREQNPX interface is not used. The PEREQ signals are directly connected between the 286 and 287, completely bypassing the VL82C320.

CPU Ready Control

On reads or writes to the 387SX, the VL82C320 automatically asserts –READYO after one wait state time-out unless the –READYI line to the VL82C320 is asserted. This prevents a system hang-up when a coprocessor is not present.

DEDICATED INTERNAL CONTROL REGISTERS

All Special Features (SF) decodes are between E8h and FFh as shown in Table 10. While the IBM Technical Reference Manual considers F8h to FFh reserved for coprocessor use, only F8h, FAh, FCh, and FEh are actually used. SF sandwiches some registers in this region. The recommended method is to decode the F8h to FFh range then AND with address bit –A0. This properly maps only the even addresses in this range to the coprocessor. I/O ports F0h and F1h are fully decoded due to the presence of other ports at F4h and F5h. It is possible to disable the SF functions mapped in the FXh range if they conflict with a specific design implementation. This feature is described later in this specification.

Note: The dedicated I/O registers at E8h, EAh, and E9h are described separately in the "EMS Subsystem" section. The dedicated I/O registers at ECh and EDh are described in the "Functional Summary of Indexed Registers" section.

TABLE 10. DEDICATED I/O CONTROL REGISTERS

Port Address	Function
E8h	EMS Index Register
E9h	EMS Active Set
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh	Fast A20* **
EFh	Fast Reset* **
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h	Slow CPU**
F5h	Fast CPU**
F8h	Coprocessor
F9h	Configuration Disable**
FAh	Coprocessor
FBh	Configuration Enable**
FCh	Coprocessor
FEh	Coprocessor

* Also can be activated through port 92h for PS/2-compatibility.

** These decodes can be disabled in case of conflict.

Note: All I/O accesses to the above registers must be byte size except the EMS data port at EAh and EBh which may be either byte or word operations.

EMS Register Set (I/O Address E9h)

E9h	D7	D6	D5	D4	D3	D2	D1	D0
EMS Register Set	X	X	X	X	X	X	X	X

A read of this address returns FFh. A read of this register activates the standard EMS register set. A write activates the alternate EMS register set. Neither of these actions has any effect if the EMS subsystem has not been enabled by setting the EMS enable bits in the EMSEN registers described in the "EMS Subsystem" and "Functional Summary of Indexed Registers" sections. Default on reset is the standard register set.

Note that this function has no relationship and is totally independent of the control afforded by bit 7 of register E8h. Bit 7 controls which register set is selected for updates to the base addresses for the EMS translation. It is possible to select and update either the standard or alternate EMS register set independent of which set is currently active. After a write to port F9h when MISCSET7 = 0, E9h becomes read-only until a write to port FBh is performed.

Fast A20 (I/O Address EEh or 92h)

EEh	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	X	X	X	X	X	X	X	X

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	CTRL	Reset

A read of I/O port EEh enables Fast A20 and returns a value of FFh. A write disables Fast A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. Internally, this signal and A20GATE are ORed so that either event controls the A20 address line and generates –BLKA20. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the A20 input for strict PC/AT-compatibility.

Fast A20 is also controlled via bit 1 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 1 = 1, A20 is active. When bit 1 = 0, A20 always = 0. This feature is fully integrated with the Fast A20 control achieved through EEh, i.e., a read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

After a write to port F9h when MISCSET7 = 0, EFh becomes read-only until a write to port FBh is performed. If MISCSET7 = 1, EEh can not be read or written.

FAST CPU Reset (I/O Address EFh or 92h)

EFh	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

This register provides an alternative to the use of the –RC input in order to reset the processor. A read of EFh resets the processor. This reset signal must be ORed internally with the –RC input so that either event invokes a reset. This may provide a faster way for the system to jump between real and protected mode. Reset timing is the same as described below for Port A reset.

Fast CPU reset can also be controlled via bit 0 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 0 = 1, a reset operation is triggered. Reset pulses are high for 16 CLK2s. This latch remains set until written again or until the VL82C320 is externally reset.

After a write to port F9h when MISCSET7 = 0, EFh becomes read-only until a write to port FBh is performed. If MISCSET7 = 1, EFh can not be read or written.

Note that in order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low, otherwise, the reset vector is not fetched and the system hangs up. Therefore, before issuing a "Hot" reset command, either via I/O port 92H or I/O port EFh as described above, one of the following must occur:

1. Set bit 1 to 1 in Port A. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.)
2. Perform a read of EEh to enable A20.

Coprocessor Control (I/O Address 0F0h and 0F1h)

0F0h	D7	D6	D5	D4	D3	D2	D1	D0
Clear/Busy	X	X	X	X	X	X	X	X

0F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Copro	X	X	X	X	X	X	X	X

A write to I/O port F0h clears the D-flop which holds –BUSYCPU and PEREQCPU active after an –ERRORNPX signal occurs. A write to I/O port F1h resets the NPX. This write results in a positive pulse 80 CLK2 cycles wide and is synchronized to CLK2. –READYO is held inactive during this entire period for 100 CLK2s after the falling edge of RESNPX.

Bit 6 of MISCSET must be set to 0, otherwise, a write to F1h does not cause a reset.

CPU Speed (I/O Address 0F4h and 0F5h)

0F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU Speed	X	X	X	X	X	X	X	X

0F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU Speed	X	X	X	X	X	X	X	X

A write to port 0F5h causes the CPU to run at normal "fast" speed. A write to port 0F4h invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET register described later in this document. The programmable range provided allows 12 to 25 MHz systems to run at or below 8 MHz. Default on reset is "fast" speed.

After a write to port F9h when MISCSET7 = 0, F4h and F5h can not be written and are effectively disabled until a write to port FBh is performed. If MISCSET7 = 1, EEh can not be read or written. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details. The speed control activated by the BIOS through the keyboard controller is always available to access this function.

Configuration Enable/Disable Registers (I/O Addresses 0FBh and 0F9h)

0FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

0F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described above, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 0FBh enables the configuration registers. A write to 0F9h disables the configuration registers. When disabled, the registers in range E8h to EFh are read-only except for E8h and ECh which remain read/write. This allows the EMS data registers and the configuration registers to be read but not modified. The fast and slow CPU speed functions controlled by writes to F4h and F5h are also disabled.

If bit 7 of the MISCSET register = 1, the configuration enable/disable feature is disabled. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details.

Sleep Mode Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP (13)	Enable	Power Down CLK2 Divider			Reserved	Reserved	Ext Ctrl 1	SYSCLK

Sleep mode operation is provided for battery operated laptop microcomputer support. The sleep indexed configuration register is provided to control this function. Bits 0 and 4 through 6 are set with the desired values by the BIOS during POST. Only bit 7 needs to be toggled to get in and out of sleep mode during operation. For maximum power savings, it is recommended that a halt instruction be executed immediately after setting bit 7.

Bit 7 is set to 1 to invoke all chip set sleep functions. When set, CLK2 is divided by the value coded in bits 4-6 of the sleep register except during HLDA cycles. These bits provide a code used to divide the CLK2 input for generation of CLK2 output during sleep mode. Division from 1 to 1024 is programmable. The range is specified in the "Functional Summary of Indexed Registers" section.

When used with non-static CPU's the greatest division is selected that allows CLK2 to remain above the minimum operational frequency.

Normally, –RAS-only refresh is performed. This requires driving the memory address lines and power is consumed. When bit 7 =1, the refresh controller may switch to –CAS before –RAS refresh. If –CAS before –RAS refresh is not desired while in sleep mode, setting CTRL1 bit 6 to 1 maintains standard refresh operation.

The VL82C320 is brought out of sleep mode by resetting bit 7 to a logic 0. This is done by providing a CPU write of 0 to bit 7. A hardware reset or an INTA cycle of the VL82C320 also resets this bit.

Bits 3 and 2 - Reserved for use by external sleep control circuitry that wishes to use the same port address for logical consistency. The internal bits are read/write, but perform no other function at the present time.

Bit 0 - The sleep register is "shadowed" in the Bus Controller. That is, it exists at the same address as a write-only register in the Bus Controller. However, only bits 0 and 7 are valid in the Bus Controller. See the VL82C331 ISA Bus Controller data sheet for more details. In the VL82C320, bit 0 is a read/write bit without function. This bit is provided so that software can detect the last state written to it in the Bus Controller.

When CTRL1 bit 0 = 0, the –SLP/MISS (pin 6) provides an external indication of the inverse state of the SLEEP bit 7. That is, when pin 6 is low, sleep mode is active. This can be used as an external indicator of sleep mode or as an external sleep mode activation signal for other devices.

See the section "Sleep Mode Operation" in the VL82C331 ISA Bus Controller data sheet and the section "Functional Summary of Indexed Registers" in this data sheet for additional information.

TURBO/Slow CPU Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET 14	FX Enable	F1 Ctrl	SD Drive	Slow CLK2 Divider	Bus CLK Divider	Bus Mode

It has become standard for fast PC/AT-compatibles to provide means to slow operation of older, speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. Bits 3-4 of the MISCSET indexed configuration register are used to specify a CLK2 divider that is active when the slow CPU mode is activated. This range provides the capability to operate at 8 MHz or under, for any actual CPU speed from 12 to 25 MHz.

One way this mode may be toggled on and off is by external control of the TURBO input pin. When TURBO is low, the slow mode is activated and the CLK2 divider is in effect. When TURBO is high or during HLDA cycles, CLK2 runs at the same speed as TCLK2 (only if the SF TURBO request is also active, see above). The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a "hot key" combination such as Ctrl Alt +. This input is often externally ANDed with a mechanical turbo switch on the front panel.

For SF compatibility, another method is provided if separately enabled. A write to I/O port 0F4h also selects the CLK2 divider circuit for slow operation. A write to 0F5h returns to full speed operation. The SF must be enabled (bit 7 of MISCSET = 0) for the latter mechanism to be active. The SF internal speed control mechanism is ANDed with the TURBO input pin. In this way, any single request for slow operation causes it to occur.

Note: The state of TURBO has no impact on the slot clock frequency. See the sections "Functional Summary of Indexed Registers" and "Dedicated Internal Control Registers" for additional data.

SPECIAL CYCLES

HALT/SHUTDOWN DETECTION

The VL82C320 detects and responds as described below to halt and shutdown operations from the 286 and 386SX processors.

The chip set detects halt only to differentiate it from the shutdown cycle. No further action is taken in response to halt except to acknowledge it by asserting –READYO after two wait states.

Shutdown is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. The VL82C320 responds by asserting –READYO after two wait states then issuing a CPU-only reset for 16 CLK2 cycles.

COPROCESSOR CYCLES

The VL82C320 generates a –READYO signal in one wait state if the –READYI is not activated prior to this when it is in the 386SX mode. In 286 mode, coprocessor cycles are run as on-board slot bus cycles under control of the ISA Bus Controller. See Coprocessor Controller Subsection for more details.

SYSTEM RESET OPTIONS

This section describes all reset modes of the VL82C320 based on their activating signal. They have been discussed in other applicable sections of this document and are summarized as an aid to the reader.

RSTDRV: Hardware reset pin from the Bus Controller. This signal causes all internal state machines to be reset. The internal configuration registers are reset to their default values shown in Table 15. Resets are issued to the CPU and the NPX. The –BUSYCPU signal is active for at least eight CLK2 cycles before and after the falling edge of the RESCPU signal. This invokes the self-test mode of the 386SX. Systems that desire to use this feature can then read the result of this test in the 386SX's EAX register and decide what to do based on the result. Otherwise, it can be ignored. This has no effect on 286-based systems.

–RC: When active, a CPU-only reset is issued immediately on RESCPU for 16 CLK2 cycles synchronous with CLK2.

REG_92: Setting bit 0 of I/O port 92h causes a CPU-only reset. After approximately 6.75 µs, a RESCPU is activated for 16 CLK2 cycles. See the section "Dedicated Internal Control Register" for more details.

REG_EF: A read of I/O port EFh causes a CPU-only reset. After approximately 6.75 µs a RESCPU is activated for 16 CLK2 cycles. SF must be enabled for this feature to function. See the section "Dedicated Internal Control Register" for more details.

TABLE 11. 286 HALT/SHUTDOWN DETECTION

M/–IO	–S1	–S0	A1	Mode
1	0	0	1	Halt
1	0	0	0	Shutdown

TABLE 12. 386SX HALT/SHUTDOWN DETECTION

M/–IO	D/–C	W/–R	A1	Mode
1	0	1	1	Halt
1	0	1	0	Shutdown

OUT_F1: A write to I/O port F1h causes an NPX-only reset. RESNPX is activated for 80 CLK2 cycles. Ready assertion is held off for another 100 CLK2 cycles. See the section "Dedicated Internal Control Registers" for details.

SHUTDOWN: Detection of the shutdown condition causes a CPU-only reset for 16 CLK2 cycles. See the section "Halt/Shutdown Detection" for additional information.

DATA BUFFER OPERATION

The VL82C320 data buffer functions separates the data bus into three buses, D bus, SD bus and the XD bus. The D bus is the CPU's local data bus. The VL82C320 and numeric coprocessor are connected to the D bus. BIOS ROMs are connected to the D Bus (16-bit) or the XD bus (8-bit). The SD bus is the 16-bit slot bus and the XD bus is an 8-bit bus for on-board peripherals such as the VL82C320 registers and the ISA Bus Controller. These buses can be controlled by either the CPU, a DMA Controller or a Bus Master. Table 13 shows the source and destination buses for all possible steering functions.

In addition, the VL82C320 provides a D bus latching mechanism. The read data from the appropriate bus (D, SD, SC) is latched and re-driven to the D bus from the end of the controlling strobe (CAS, IOR, MEMR) to the point at which the CPU samples the data.

ROM CYCLES

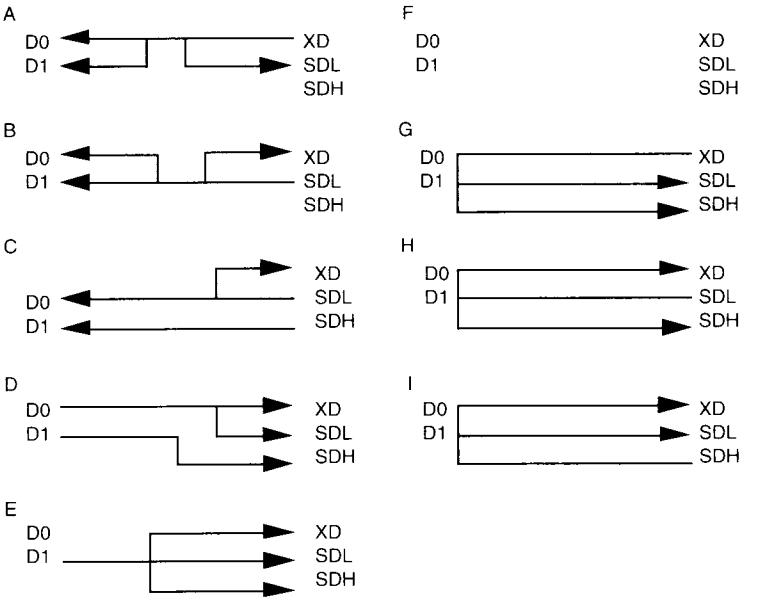
With power-on reset defaults, two address regions result in generation of –ROMCS and access of data on the D bus for 16-bit ROM systems or the XD bus for 8-bit ROM systems. These are:

1) 000E0000h - 000FFFFFh
   Accesses can be altered via EAXS, FAXS, EMSEN1, or RAMSET7. See detailed discussions of these actions elsewhere in the data sheet.

2) 00FE0000h - 00FFFFFFh
   Accesses to this region can not be disabled. In systems with 16-32M of on-board DRAM, DRAM in this 128K region is only accessible via the EMS registers.

TABLE 13. DATA BUFFER MODE SUMMARY

		TO D BUS		TO S BUS		
		D0	D1	XD	SDL	SDH
FROM D BUS	D0	F		D	D	
	D1		F	E	E	D E
FROM S BUS	XD	A	A		G	G
	SDL	B C	B	H	F	H
	SDH		C	I	I	F



Timing of ROM cycles is handled by the VL82C331 ISA Bus Controller. See the "ROM Access Control" subsection paragraph of that specification for further information.

PARITY GENERATION AND DETECTION CIRCUIT

System board memory write cycles generate two parity bits, one for each byte of the 16-bit word bank. These bits are written out coincident with the data write. On CPU reads both system board DRAM bytes feed the parity checker. In case of a parity error, the –PARERROR line is activated to the Bus Controller.

IN-CIRCUIT TEST DESCRIPTION

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
CLK2IN	2	D13	14
–READYI	3	HRQ	8
HLDA	4	PEREQCPU	11
–READYO	7	D15	12
RESCPU	8	D14	13
PAR1	21	D0	29
PAR0	30	D1	28
PEREQNPX	68	–ROMCS	63
ERRORNPX	69	–REFRESH	64
–BUSYNPX	70	IRQ13	66
TCLK2	71	–NPCS	67
286/–386SX	78	XD5	103
–CHREADY	80	XD6	102
DMAHRQ	83	–BRDRAM	99
OUT1	84	BUSCLK	97
–IOR	85	CHM/–IO	95
–IOW	86	–CHS0/–MW	93
SDLH/–HL	88	XD7	101
–SDSWAP	89	–CHS1/–MR	94
–XDREAD	90	–BLKA20	96
–LATLO	91	DMAHLDA	98
–EALE	92	–PARERROR	100
A16	139	SD6	123
A17	138	SD4	125
A18	137	SD2	128
A19	136	SD1	129
A20	135	SD0	130
A21	134	SD3	127
A22	133	SD5	124
A23	132	SD7	122
–ADS	160	CLK2	5
M/–IO	159	–BUSYCPU	10
D/–C (–S1)	158	–SLP/MISS	6

IN-CIRCUIT TEST LOGIC

The VL82C320 is designed to make system board testing as easy as possible. The –TRI input causes all pins on the VL82C320 go to a high impedance state. This can be used to isolate the VL82C320 so other components in the system can be tested.

The –TRI input can also be used to put the VL82C320 into a special test mode called In-Circuit Test (ICT). The purpose of ICT is not to functionally test the VL82C320 while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern.

During In-Circuit Test (ICT), each output may be toggled by one or more of the inputs. This allows for a board level tester to check the solder connection of each pin. The sequence for enabling ICT is as follows:

1. Tester drives –TRI pin low.
2. Tester drives XD0 with a value of 1.
3. Tester simultaneously pulses –IOR and –IOW low for at least 100 ns.
4. Tester drives –TRI pin high.
5. VL82C320 remains in ICT mode until the RSTDRV pin is activated or until steps 1-4 are repeated with XD0 = 0.

ICT INPUT		ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
MA10	33	–RAMWR	48	D12	15
MA9	3	–RASBK3	59	D11	16
MA8	35	–RASBK2	60	D10	17
MA7	37	–CAS7	49	D9	18
MA6	38	–CAS6	50	D8	20
MA5	39	–CAS5	51	D7	22
MA4	40	–CAS4	52	D6	23
MA3	43	–CAS3	53	D5	24
MA2	44	–CAS2	54	D4	25
MA1	45	–CAS1	56	D3	26
MA0	47	–CAS0	57	D2	27
A1	154	A15	140	SD8	119
A2	153	A14	141	SD9	118
A3	152	A13	142	SD10	117
A4	151	A12	143	SD11	116
A5	150	W/–R (–S0)	157	SD12	114
A6	149	–BLE (A0)	156	SD13	113
A7	148	–BHE	155	SD14	112
A8	147	–RASBK1	61	SD15	111
A9	146	–RASBK0	62	XD0	109
A10	145	RESNPX	65	XD1	107
A11	144	OSC	72	XD2	106
BUSOSC	73	TURBO	76	XD3	105
A20GATE	75	–RC	77	XD4	104

CONFIGURATION REGISTER SET
Software Access
Index Registers (I/O Address ECh)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address EDh. All subsequent data port reads and writes access the register at this address until the index register is written with a new 8-bit address. This register is readable. It always returns the last value written to it.

The Configuration Registers can only be accessed via the CPU and are limited to byte reads and writes.

Data Port Register (I/O Address EDh)
Each register accessible through I/O address EDh is functionally described below. It is accessed first by writing its address to the index register at I/O address ECh, then by accessing the data port at I/O address EDh.

FUNCTIONAL SUMMARY OF INDEXED REGISTERS
Version (00h) (Read-only)
D2-D7 contains a read-only code which indicates that this part is a VLSI Technology PC/AT-compatible System Controller/Data Buffer (VL82C320). D0 and D1 contain the version number of this chip. The first version of this chip uses the code E0h. Breaking the code into two bit pieces reveals it to be "320" Rev "0."

COMPAT (01h)
Bits 7-0 are read-only and always return to logic 1's. This register is included for compatibility with the Bus Controller.

SLTPTR (02H) (Default = FFh)
The SLTPTR register represents the upper address bits of the base address where off-board (slot) memory accesses begin. It contains a full 8 bits corresponding to A16-A23. (For more details, see "SLTPTR - Critical Memory Control Element" section.)

RAMMAP (03h) (Default = E0h)
Bit 7 in conjunction with the EAXS register determines system response to memory accesses between 0E0000h-0EFFFFh. When set to a logic 1 and the EAXS code for the specific 16K segment is 00b, reads generate a –ROMCS and a ROM access is performed from either the D or XD bus depending on whether 8- or 16-bit ROM BIOS is used. When set to logic 0 and the EAXS code for the specific 16K segment is 00b, reads and writes are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in the 0E0000h-0EFFFFh area. See EAXS below for further details. Accesses to the area between FE0000h-FEFFFFh also respond in the above manner except that EAXS has no control over this memory space.

Bits 4-0 specify one of the valid memory maps as shown in Table 1. Note that not all possible 5-bit codes are assigned to valid memory maps.

RAMMOV (04h) (Default = F0h)
Bits 3-0 specify a switching function which determines which internal –RASBK3 - –RASBK0 signals drive which external –RASBK3 - –RASBK0 pins.

Refer to Table 2 for the REMAP configuration register code mapping.

RAMSET (05h) (Default = 3Ch)
Bits 7-6 program the drive current on lines MA0-MA10 and on –RAMW according to the following codes:
00 = 150 pF drive (Default)
01 = 300 pF drive
10 = 450 pF drive
11 = 600 pF drive

Bit 5 is set to 0 in order to allow a cycle to begin one CLK2 earlier. This provides extra access time. (Default = 1 Early Start Disable.) Early Start may be enabled in systems running at 20 MHz or below.

Bit 3 indicates whether page mode is active on Bank A.
0 = disabled
1 = enabled (Default)

Bit 2 indicates whether page mode is active on Bank B.
0 = disabled
1 = enabled (Default)

Bit 1 indicates the interleave mode for Bank A.

0 = Interleave on bit 1 for all DRAMs (Default)

1 = Interleave on bit 10 for all DRAMs

Bit 0 indicates the interleave mode for Bank B.

0 = Interleave on bit 1 for all DRAMs (Default)

1 = Interleave on bit 10 for all DRAMs

REFCTL (06h) (Default = 00h)
Bit 3 controls internal I/O decode. When bit 3 = 0, full 16-bit decode is performed. When bit 3 = 1, 10-bit decode is performed. (Default = 0.)

Bits 2-0 specify a divider applied to the OUT1 timing pulse for slowing the DRAM refresh from its nominally programmed rate.
000 = ÷ 1 (Default)
001 = ÷ 2
010 = ÷ 4
011 = ÷ 8
100 = ÷ 16

RASTMA - RAS Timing for DRAM Banks 0 and 1 (07h) (Default = FFh)
Bit 7 indicates the –RAS to Column Address delay.
0 = 1/2 CLK2
1 = 1 CLK2 (Default)
Refer to Figure 4.

Bit 6 indicates number of clock delays between –RAS and –CAS (tRCD). Actual clock delays encoded by this bit are:
0 = 1 CLK2
1 = 2 CLK2s (Default)
Refer to Figure 2.

Bits 4-3 indicate the number of clock periods of –RAS precharge time (tRP). Bit encoding relative to the number of clocks is:
00 = 2 CLK2s
01 = 3 CLK2s
10 = 4 CLK2s
11 = 5 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 longer than programmed.

Bits 2-0 indicate the number of clock periods of –RASBK active time (tRAS). Bit encoding relative to the number of clocks is:
010 = 2 CLK2s
011 = 3 CLK2s
100 = 4 CLK2s
101 = 5 CLK2s
110 = 6 CLK2s
111 = 7 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 shorter than programmed.

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CASTMA - CAS Timing for DRAM Banks 0 and 1 (08h) (Default = B7h)
Bits 7-6 indicate the number of clock cycles of –CAS active time during memory writes (tCASW):
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s (Default)
11 = 4 CLK2s
Refer to Figure 2.

Note: In 286 mode, these times may be on half CLK2 shorter than programmed.

Bit 5 indicates the number of CLK2s of delay that occur before –CAS goes active after the start of the status cycle (tCST). This parameter is applicable to write operations only.
0 = 3 CLK2s
1 = 4 CLK2s (Default)
Refer to Figure 3.

Bits 4-3 indicate the number of clock cycles of –CAS precharge time (tCP). Bit encoding relative to the number of clocks is:
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 longer than programmed.

Bits 1-0 indicate the number of clock cycles of –CAS active time during memory reads (tCASR). Bit encoding relative to the number of clocks is:
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)
00 = 5 CLK2s
Refer to Figure 2.

Note: In 286 mode, these times may be on half CLK2 shorter than programmed.

RASTMB - RAS Timing for DRAM Banks 2 and 3 (09h) (Default = FFh)
See RASTMA for bit definitions.

CASTMB - CAS Timing for DRAM Banks 2 and 3 (0Ah) (Default = B7h)
See CASTMA for bit definitions.

EMSEN1 (0Bh) (Default = 00h)
Bit 7 is set as global enable for the EMS translation registers from C0000h to EC000h.
0 = EMS disable (Default)
1 = EMS enable

Bit 6 is set as the global enable for the EMS backfill translation registers from 40000 to 9C000h.
0 = Backfill Disable (Default)
1 = Backfill Enable

Bit 4 determines the EMS window range.
0 = EMS Map 0
1 = EMS Map 1

Each bit below is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 8
Bit 1	EMS Page 9
Bit 2	EMS Page 10
Bit 3	EMS Page 11

EMSEN2 (0Ch) (Default = 00h)
Each bit is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 0
Bit 1	EMS Page 1
Bit 2	EMS Page 2
Bit 3	EMS Page 3
Bit 4	EMS Page 4
Bit 5	EMS Page 5
Bit 6	EMS Page 6
Bit 7	EMS Page 7

SHADOW CONTROLLER REGISTERS (Default = 00h)
The following registers provide control over the memory range from 640K to 1 Mbyte. Each pair of bits control one 16K page as defined below:
00 = Read (Default), Write Slot Bus
01 = Read (Default), Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

*In the address space F0000h to FFFFFh, Default means accesses are from on-board ROM space. Default accesses in areas from A0000h-DFFFFh are from the slot bus. Default in the area from E0000h-EFFFFh can be either on-board ROM or slot bus accesses depending on the state of RAMMAP bit 7.

AAXS (0Dh) *Default is always the slot bus.
Bits 6-7 - segment at AC000h
Bits 4-5 - segment at A8000h
Bits 2-3 - segment at A4000h
Bits 0-1 - segment at A0000h

BAXS (0Eh) *Default is always the slot bus.
Bits 6-7 - segment at BC000h
Bits 4-5 - segment at B8000h
Bits 2-3 - segment at B4000h
Bits 0-1 - segment at B0000h

CAXS (0Fh) *Default is always the slot bus.
Bits 6-7 - segment at CC000h
Bits 4-5 - segment at C8000h
Bits 2-3 - segment at C4000h
Bits 0-1 - segment at C0000h

DAXS (10h) *Default is always the slot bus.
Bits 6-7 - segment at DC000h
Bits 4-5 - segment at D8000h
Bits 2-3 - segment at D4000h
Bits 0-1 - segment at D0000h

EAXS (11h) *Default may be on-board BIOS ROM access or slot bus access.
This memory space is a special case in that "default" can be one of two locations depending on the state of the RAMSET bit 7.
Bits 6-7 - segment at EC000h
Bits 4-5 - segment at E8000h
Bits 2-3 - segment at E4000h
Bits 0-1 - segment at E0000h

RAMMAP[7]	EAXS	Operation
0	00	Read/Write Slot Bus
1	00	Read On-Board ROM, Write Slot Bus (–ROMCS Active)
0	01	Shadow Setup Mode: Read Slot Bus, Write System Board
1	01	Shadow Setup Mode: Read On-Bus ROM, Write System Board
X	10	Read System Board/Write Slot Bus (Shadow Active)
X	11	Read/Write System Board

FAXS (12h) *Default is always on-board BIOS ROM access.
Bits 6-7 - segment at FC000h
Bits 4-5 - segment at F8000h
Bits 2-3 - segment at F4000h
Bits 0-1 - segment at F0000h

SLEEP (13h) (Default = 01h)
Bit 7 - Power-down enable.
0 = Default operational setting. Normal clock speed.
1 = Invokes clock divider set in bits 4-6.

This bit is reset to 0 and normal operation resumes when rewritten or when the VL82C320 receives a hardware reset.

Bits 6-4 - Power-down CLK2 divider. These bits provide a code used to divide the CLK2 down for sleep mode. The codes are:
000 = ÷1 (Default /1 clock)
001 = ÷4
010 = ÷8
011 = ÷16
100 = ÷32
101 = ÷64
110 = ÷256
111 = ÷1024

Bit 1 - External Control 1
Bit 1 along with Bit 7 control the –SLP/MISS pin.

Bit 0 is a simple latch that provides no functionality in the VL82C320. However, a read always reflects the last write to this bit.

MISCSET (14h) (Default = 06h)
When bit 7 is set to 1, the special features accesses via ports EEh, EFh, F4h, 5h, F9h, and FBh are disabled. These features are described in the "Dedicated Internal Control Registers" section earlier in this document.
0 = enabled (Default)
1 = disabled

Bit 6 controls coprocessor software reset.
0 = enabled (Default)
1 = disabled

Bit 5 is SD high drive enable.
0 = 24 mA drive (Default)
1 = 12 mA drive

Bits 4-3 specify the CLK2 divider that is invoked when the TURBO input pin is low or when a write to port F4h is performed.
00 = CLK2 ÷1 (Default)
01 = CLK2 ÷2
10 = CLK2 ÷3
11 = CLK2 ÷4

Bits 2-1 are the value used for division of TCLK2 or BUSOSC to generate BUSCLK.
00 = ÷ 1
01 = ÷ 2
10 = ÷ 3
11 = ÷ 4 (Default)

Bit 0 indicates the BUSCLK divider source.
0 = TCLK2 (Default)
1 = BUSOSC

TEST (15h) (Default = 00h)
This register is reserved for "to be determined" factory test functions. It must never be written during normal operation.

CTRL1(16h) (Default = 00h)
This register contains additional system functional controls.

Bit 7 provides for disk controller compatibility. With fast CPUs, some disks can be overrun by programmed I/O. This bit provides a way to compensate by forcing the first memory cycle after an I/O cycle to be executed at non-turbo speed.
0 = slow programmed I/O (Default)
1 = normal programmed I/O

Bit 6 selects the sleep mode refresh option.
0 = CAS before RAS refresh
1 = normal refresh

Bits 5-4 are used to open a 64K or 128K window at the top of DOS memory for access by slot bus cards. This allows accesses to be directed off-board in this region, then come back on-board in order to access on-board extended memory. The slot pointer (SLTPTR) can not be used to provide this function because all accesses above slot pointer are off-board. There is no way to gain access to on-board memory above this pointer except through the EMS hardware. These bits affect only the CPU address space from 512K-640K.
00 = 512K-640K on-board access
10 = 576K-640K accesses slot bus
512K-576K on-board accesses
11 = 512K-640K accesses slot bus

Special cases: This feature is inactive when EMS backfill is enabled. An attempt to set a code other than 00b with EMS backfill enabled will fail to change the code. If this feature is activated with codes 1Xb and EMS backfill is later activated, the code will automatically change to 00b disabling slot bus accesses in this region.

Use of SLTPTR in the same range is totally compatible. SLTPTR rules. If SLTPTR = 576K or 512K, the setting of CTRL1 bits 5 and 4 doesn't matter. Accesses will be directed to the slot bus in this region and will also remain off-board above 640K.

Bit 2 programs the drive current on outputs RASBK3-RASBK0
0 = 24 mA (Default)
1 = 12 mA

Bit 1 is read/write and reserved for future use. Do not write 1's to these bits.

Bit 0 will also be used for this future circuit but it also controls a function in this version of the VL82C320.

Bit 0 - –SLP/MISS pin
0 = –SLP (Default)
1 = MISS input

TABLE 14. INDEXED CONFIGURATION REGISTER MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	A7	A6	A5	A4	A3	A2	A1	A0

	Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1	1	1	0	0	0	0	0
01	COMPAT	1	1	1	1	1	1	1	1
02	SLTPTR	A23	A22	A21	A20	A19	A18	A17	A16
03	RAMMAP	ROMSLOT	1	1	DRAM Memory Map Code				
04	RAMMOV	1	1	1	1	RASBK - CAS Swap Code			
05	RAMSET	DRAM Drive		ESTART	1	Page Md A	Page Md B	Bank A Int	Bank B Int
06	REFCTL	0*	Reserved			10/16 IO	Refresh Divider		
07	RASTMA	RAS ADDSEL	tRCD	1	tRP		tRAS		
08	CASTMA	tCASW		tCST	tCP		1	tCASR	
09	RASTMB	RAS ADDSEL	tRCD	1	tRP		tRAS		
0A	CASTMB	tCASW		tCST	tCP		1	tCASR	
0B	EMSEN1	EMS Enable	BF Enable	Reserved	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
0C	EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
0D	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0E	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0F	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13	SLEEP	Enable	Power Down CLK2 Divider			Reserved	Reserved	Ext Ctrl 1	SYSCLK
14	MISCSET	FX Enable	F1 Ctrl	High Drive	Slow CLK2 Divider		Slot Bus Divider		Bus Mode
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	DSKTMG	SLPREF	512-640K Access		Reserved	RASDRV	Reserved	PRESNT

* Always write a 0 to bit D7.

Note: A 1 indicates currently unused bits that read back as logic 1. It is recommended that they be written as a "1" to ensure future compatibility.

TABLE 15. DEFAULT CONFIGURATION VALUES AFTER RESET

Data Port EDh (R/W)		D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1R	1R	1R	0R	0R	0R	0R	0R
01	COMPAT	1R	1R	1R	1R	1R	1R	1R	1R
02	SLTPTR	1	1	1	1	1	1	1	1
03	RAMMAP	1	1R	1R	0	0	0	0	0
04	RAMMOV	1R	1R	1R	1R	0	0	0	0
05	RAMSET	0	0	1	1R	1	1	0	0
06	REFCTL	0	0	0	0	0	0	0	0
07	RASTMA	1	1	1R	1	1	1	1	1
08	CASTMA	1	0	1	1	0	1R	1	1
09	RASTMB	1	1	1R	1	1	1	1	1
0A	CASTMB	1	0	1	1	0	1R	1	1
0B	EMSEN1	0	0	0	0	0	0	0	0
0C	EMSEN2	0	0	0	0	0	0	0	0
0D	AAXS	0	0	0	0	0	0	0	0
0E	BAXS	0	0	0	0	0	0	0	0
0F	CAXS	0	0	0	0	0	0	0	0
10	DAXS	0	0	0	0	0	0	0	0
11	EAXS	0	0	0	0	0	0	0	0
12	FAXS	0	0	0	0	0	0	0	0
13	SLEEP	0	0	0	0	0	0	0	1
14	MISCSET	0	0	0	0	0	1	1	0
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	0	0	0	0	0	0	0	0

Note: Values followed by "R" are read-only and have no logical function. Reserved bits in the Test register are for factory test.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	25	42	ns	
t2	TCLK2 High Time	10		ns	2.0 V
t3	TCLK2 Low Time	10		ns	2.0 V
t4	BUSOSC Period	20		ns	
t5	BUSOSC, OSC High Time	8		ns	1.5 V
t6	BUSOSC, OSC Low Time	8		ns	1.5 V
t7	CLK2IN High Time	8		ns	2.0 V
t8	CLK2IN Low Time	8		ns	2.0 V
tD9	TCLK2 to CLK2 Delay		25	ns	CL=50 pF
t10	CLK2 Fall Time		4	ns	3.6 V to 1.0 V @ CL=50
t11	CLK2 Rise Time		4	ns	1.0 V to 3.6 V @ CL=50
tD12	TCLK2 to BUSCLK Delay		25	ns	CL=50 pF
tD13	BUSOSC to BUSCLK Delay		25	ns	CL=50 pF
t14	BUSCLK Fall Time		9	ns	3.6 V to 1.0 V @ CL=50
t15	BUSCLK Rise Time		12	ns	1.0 V to 3.6 V @ CL=50
tD16	CLK2IN to RESCPU Delay	3	13	ns	CL=30 pF
tD17	CLK2IN to RESNPX Delay	3	13	ns	CL=30 pF
tD18	CLK2IN to –READYO Delay	4	18	ns	CL=30 pF
tD19	CLK2IN to HRQ Delay	3	20	ns	CL=50 pF
tSU20	–ADS to CLK2IN Setup Time	23		ns	
tH21	–ADS from CLK2IN Hold Time	4		ns	
tSU22	W/–R, M/–IO, D/–C to CLK2IN Setup Time	20		ns	
tH23	W/–R, M/–IO, D/–C from CLK2IN Hold Time	4		ns	
tSU24	A23-A1 to CLK2IN Setup Time	20		ns	
tH26	A23-A1 from CLK2IN Hold Time	4		ns	
tSU27	–BHE, –BLE to CLK2IN Setup Time	15		ns	
tH28	–BHE, –BLE from CLK2IN Hold Time	4		ns	
tD29	–ADS to –EALE Delay	3	17	ns	CL=50 pF
tSU30	HLDA to CLK2IN Setup Time	10		ns	
tH31	HLDA to CLK2IN Hold Time	4		ns	
tSU32	–READYIN to CLK2IN Setup Time	12		ns	
tH33	–READYIN from CLK2IN Hold Time	4		ns	
tD34	CLK2IN to –RASBK3- –RASBK0 Delay	4	16	ns	CL=150 pF
tD35	CLK2IN to –RAMW Delay	4	23	ns	CL=300 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD36	CLK2IN to –CAS7- –CAS0 Delay	4	16	ns	CL=50 pF
tD37	CLK2IN to –BRDRAM Delay	4	20	ns	CL=50 pF
tD40	CLK2IN to –ROMCS Delay	4	35	ns	CL=50 pF
tD41	A23-A1 to MA10-MA0 Delay	4	29	ns	CL=300 pF
tD42	CLK2IN to MA10-MA0 Delay	4	25	ns	CL=300 pF
tD43	CLK2IN to MA10-MA0 Delay	4	30	ns	CL=300 pF
tD46	CLK2IN to –CHS0/–MR, –CHS1/–MW CHM/–IO Going Low Delay	3	18	ns	CL=50 pF
tD47	BUSCLK to –CHS0/–MR, –CHS1/–MW, CHM/–IO Going High Delay	3	22	ns	CL=50 pF
tSU48	–CHREADY to BUSCLK Setup Time	5		ns	
tH49	–CHREADY from BUSCLK Hold Time	7		ns	
tSU50	D15-D0 to –IOW High Setup Time	30		ns	
tH51	D15-D0 from –IOW High Hold Time	15		ns	
tD52	–IOR Low to D15-D0 Delay	5	50	ns	CL=50 pF
tD53	–IOW High to –SLP/MISS Delay	4	33	ns	CL=50 pF
tD54	A20GATE to –BLKA20 Delay	4	20	ns	CL=50 pF
tD56	–IOW or –IOR Low to –BLKA20 Delay	5	25	ns	CL=50 pF
tSU57	DMAHRQ to BUSCLK Setup Time	10		ns	
tH58	DMAHRQ from BUSCLK Hold Time	8		ns	
tD59	BUSCLK to DMAHLDA Delay	3	30	ns	CL=50 pF
tD60	CLK2IN to DMAHLDA Delay	3	26	ns	CL=50 pF
tD61	BUSCLK to –REFRESH Delay	3	32	ns	CL=200 pF
tD62	CLK2IN to –REFRESH Delay	3	32	ns	CL=200 pF
tD63	BUSCLK to –REFRESH Float Delay	3	20	ns	
tD66	–ERRORNPX Low to IRQ13 Delay	3	20	ns	CL=50 pF
tD67	–IOW Low to IRQ13 Low Delay	3	35	ns	CL=50 pF
tD68	PEREQNPX to PEREQCPU Delay	3	20	ns	CL=50 pF
tD69	–BUSYNPX High to PEREQCPU High Delay	3	30	ns	CL=50 pF
tD70	–IOW Low to PEREQCPU Low Delay	3	35	ns	CL=50 pF
tD71	–BUSYNPX to –BUSYCPU Delay	3	30	ns	CL=50 pF
tD72	–IOW Low to –BUSYCPU Delay	3	35	ns	CL=50 pF
tD73	CLK2IN to –BUSYCPU Delay	3	23	ns	CL=50 pF
tD74	CLK2IN to –NPCS Delay	3	23	ns	CL=50 pF
tSU75	RSTDRV to CLK2IN Setup Time	10		ns	
tH76	RSTDRV from CLK2IN Hold Time	5		ns	
tD77	CLK2IN to D15-D0 Driven Delay	3	25	ns	CL=50 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD78	CLK2IN to D15-D0 Float Delay	3	20	ns	CL=50 pF
tD79	CLK2IN to PAR1-PAR0 Driven Delay	3	25	ns	CL=50 pF
tD80	CLK2IN to PAR1-PAR0 Float Delay	3	25	ns	CL=50 pF
tD81	CONTROL to SD15-SD0 Driven Delay	3	25	ns	
tD82	CONTROL to SD15-SD0 Float Delay	3	25	ns	
tD83	–XDREAD High to XD Driven Delay	3	25	ns	
tD84	–XDREAD Low to XD Float Delay	3	25	ns	
tSU85	SD7-SD0, XD7-XD0, D7-D0 to –LATLO Setup	15		ns	
tH86	SD7-SD0, XD7-XD0, D7-D0 from –LATLO Hold	5		ns	
tSU87	SD15-SD0, XD7-XD0, D15-D8 to BUSCLK Setup	8		ns	
tH88	SD15-SD0, XD7-XD0, D15-D8 from BUSCLK Hold	15		ns	
tD89	D15-D0 to SD15-SD0 Delay		18	ns	CL=200 pF
tD90	XD7-XD0 to SD15-SD0 Delay		30	ns	CL=200 pF
tD91	SD15-SD8 to SD7-SD0 Delay		30	ns	CL=200 pF
tD92	SD7-SD0 to SD15-SD8 Delay		30	ns	CL=200 pF
tD93	D15-D0 to XD7-XD0 Delay		25	ns	CL=50 pF
tD94	SD15-SD0 to XD7-XD0 Delay		25	ns	CL=50 pF
tD95	XD7-XD0 to D15-D0 Delay		25	ns	CL=50 pF
tD96	SD15-SD0 to D15-D0 Delay		25	ns	CL=50 pF
tSU97	D15-D0, PAR1-PAR0 to CLK2IN Setup	3		ns	
tD98	D15-D0, PAR1-PAR0 from CLK2IN Hold	10		ns	
tD99	CLK2IN to –PARERROR Delay	3	32	ns	CL=50 pF
tD100	D15-D0 to PAR1-PAR0 Delay		20	ns	CL=50 pF
	OUT1, TURBO, –RC, 286/–386SX, –TRI			ns	No AC Specs on these Pins
tSU101	–CHS0/–MW, –CHS1/–MR to CLK2IN Setup	10		ns	
tH102	–CHS0/–MW, –CHS1/–MR from CLK2IN Hold	4		ns	
tD103	–CHS0/–MW to –RAMW Delay	3	25	ns	CL=300 pF
tD104	–CHS0/–MW Low to PAR1-PAR0 Driven Delay	3	25	ns	CL=50 pF
tD105	–CHS0/–MW High to PAR1-PAR0 Float Delay	3	25	ns	CL=50 pF
tD106	SD15-SD0 to PAR1-PAR0 Delay	3	30	ns	CL=50 pF
tD107	–CHS0/–MW, –CHS1/–MR to –BRDRAM Delay	3	25	ns	CL=50 pF
tD108	A23-A1 to –BRDRAM Delay	3	42	ns	CL=50 pF
tD109	–CHS0/–MW Low to D15-D0 Driven Delay	3	25	ns	CL=50 pF
tD110	A23-A1 Valid to D15-D0 Driven Delay	3	42	ns	CL=50 pF
tD111	–CHS0/–MW High to D15-D0 Float Delay	3	25	ns	CL=50 pF
tD112	A23-A1 Invalid to D15-D0 Float Delay	3	42	ns	CL=50 pF

TIMING DIAGRAMS

FIGURE 8. CLOCK TIMING

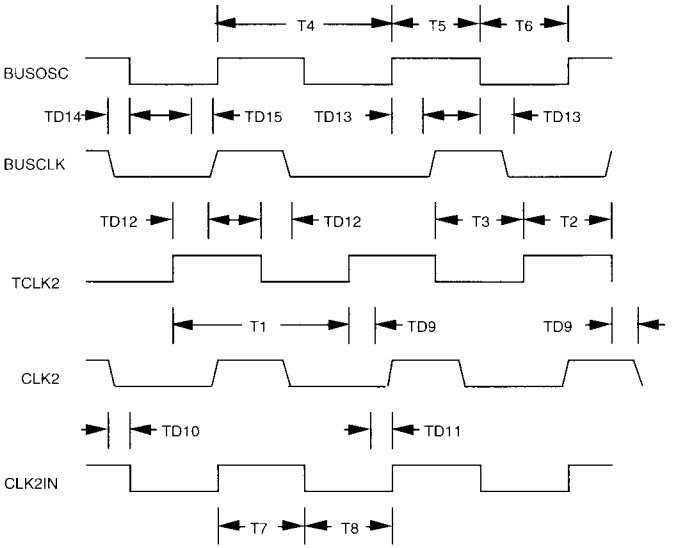

FIGURE 8A. CPU INTERFACE TIMING

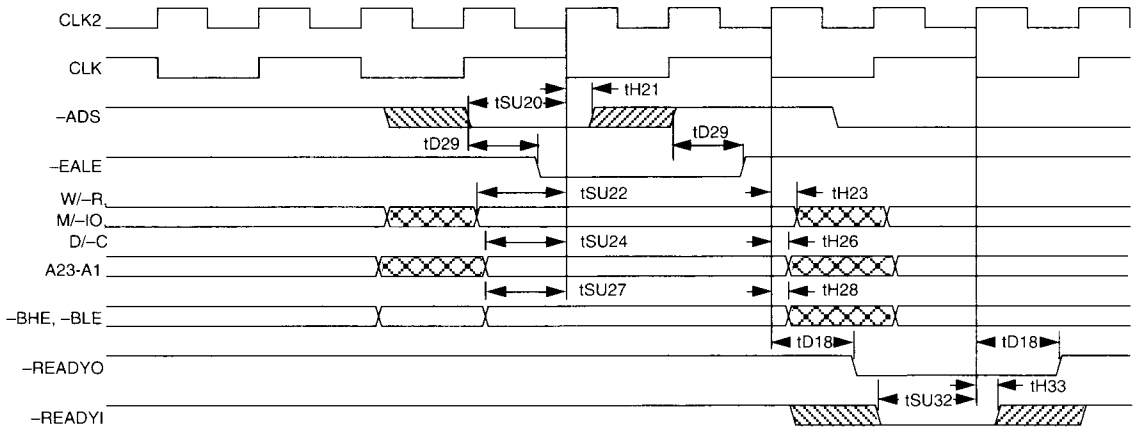

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FIGURE 9. RESET AND HOLD TIMINGS

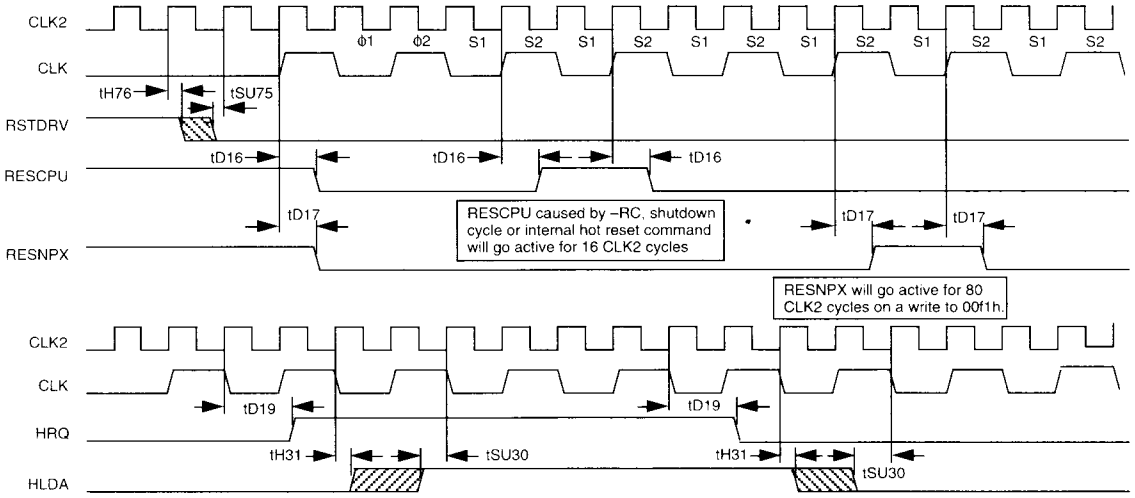

FIGURE 10. ON-BOARD MEMORY TIMING

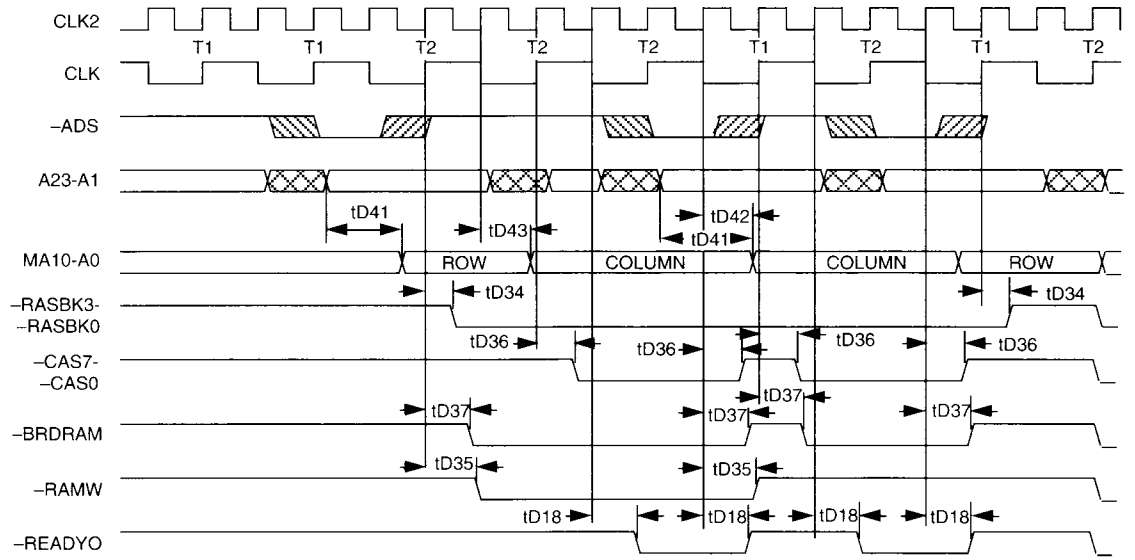

FIGURE 11. VL82C320/VL82C331 INTERFACE TIMING; A20 CONTROL TIMING

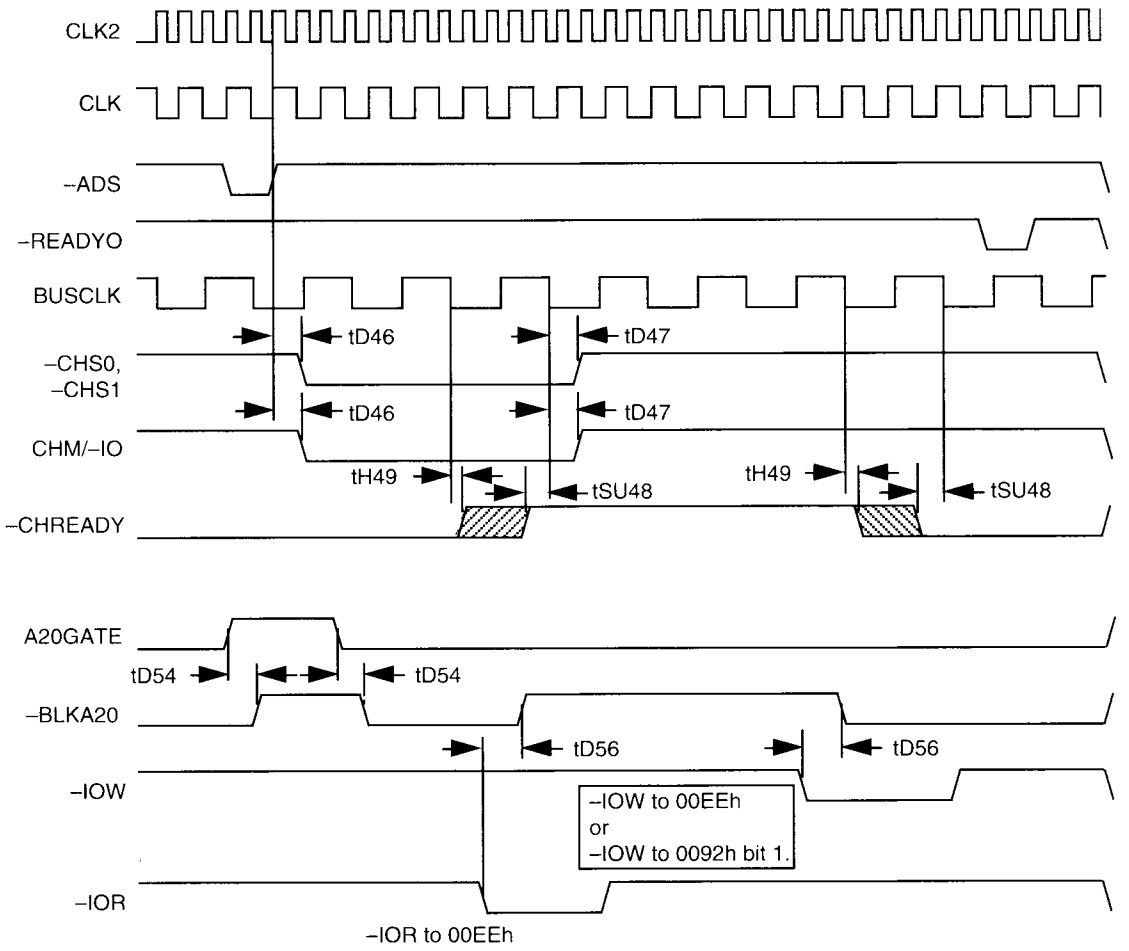

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FIGURE 12. HOLD CYCLES TIMING

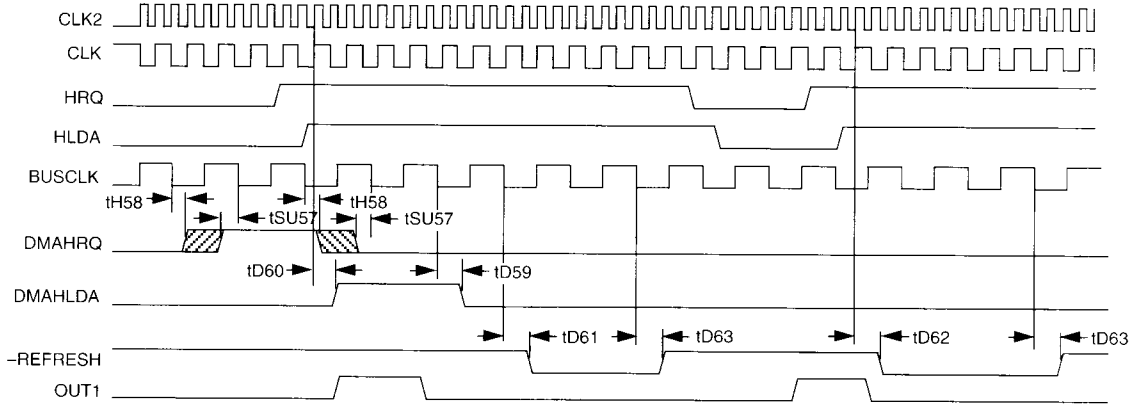


FIGURE 12A. DMA TIMING

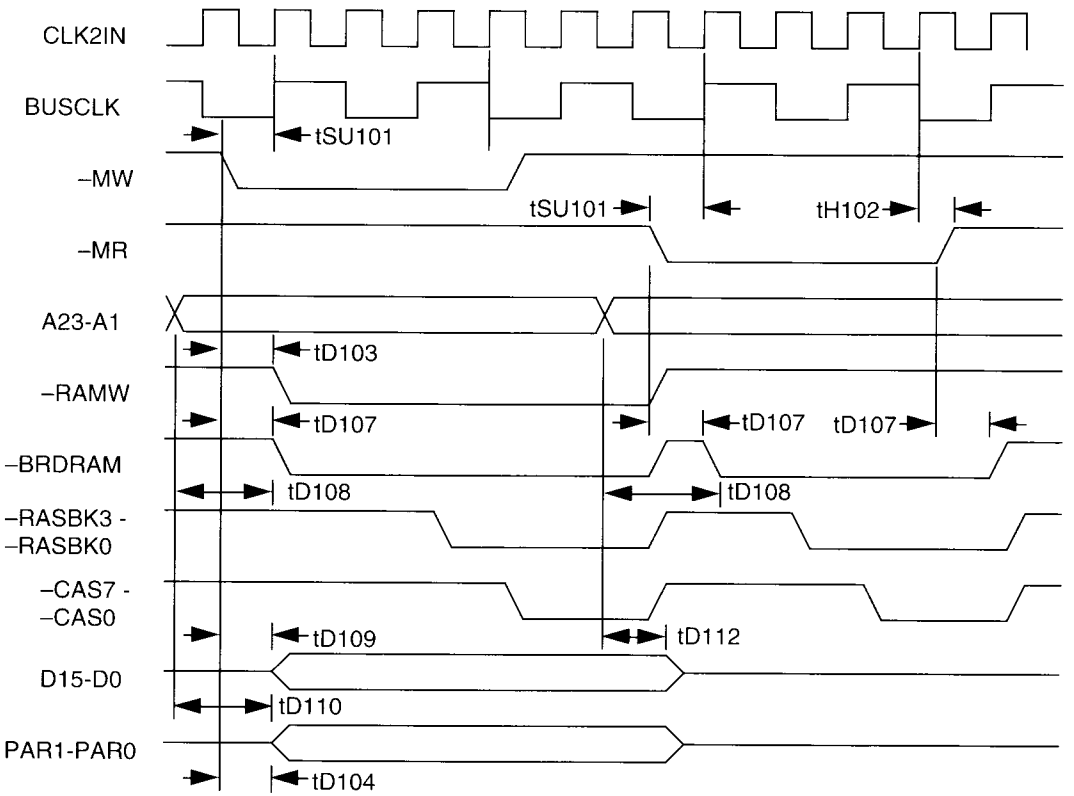


FIGURE 13. COPROCESSOR INTERFACE TIMING 386SX AND 287

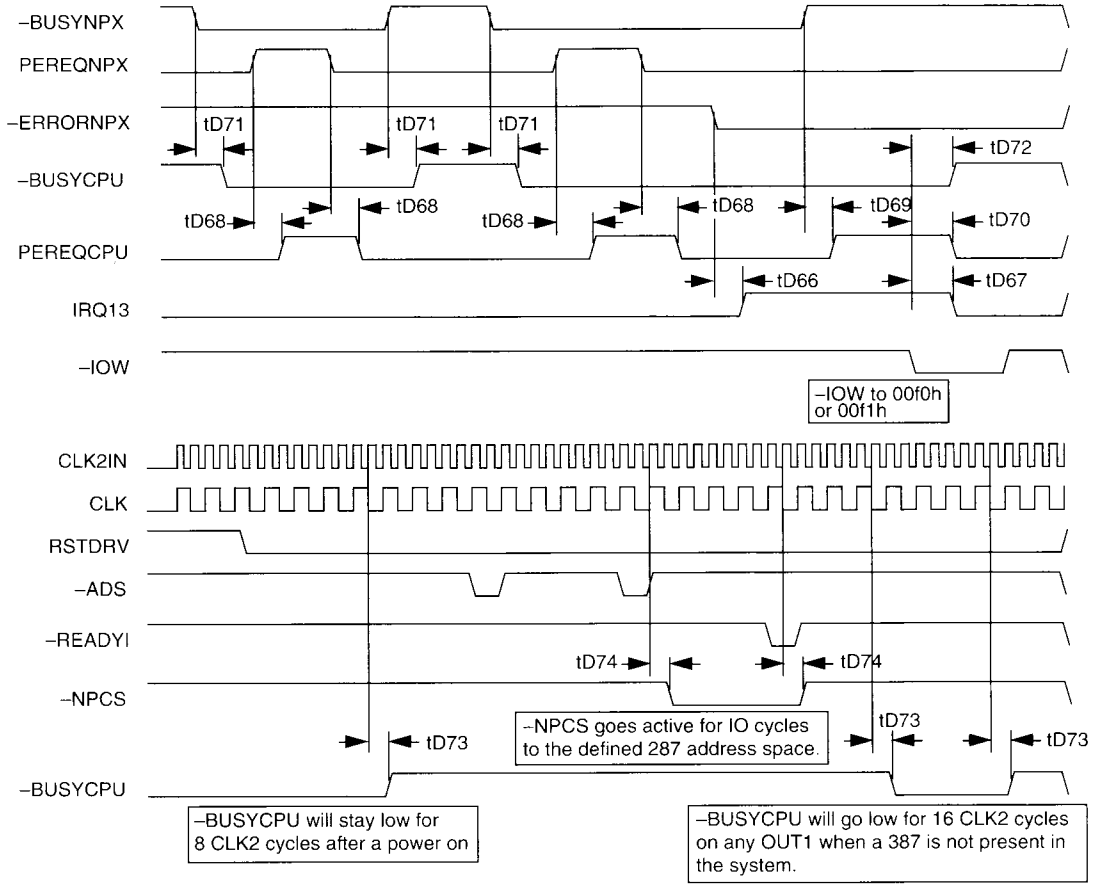


FIGURE 14. ROM CYCLE

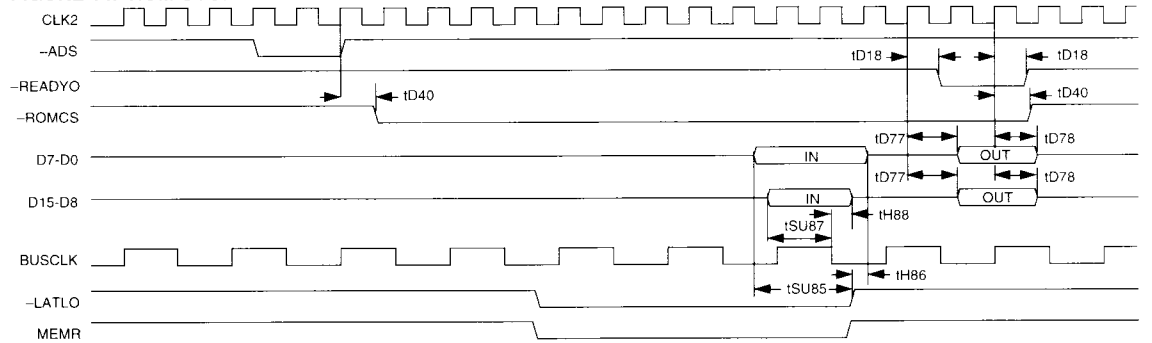


FIGURE 15. D BUS TIMINGS

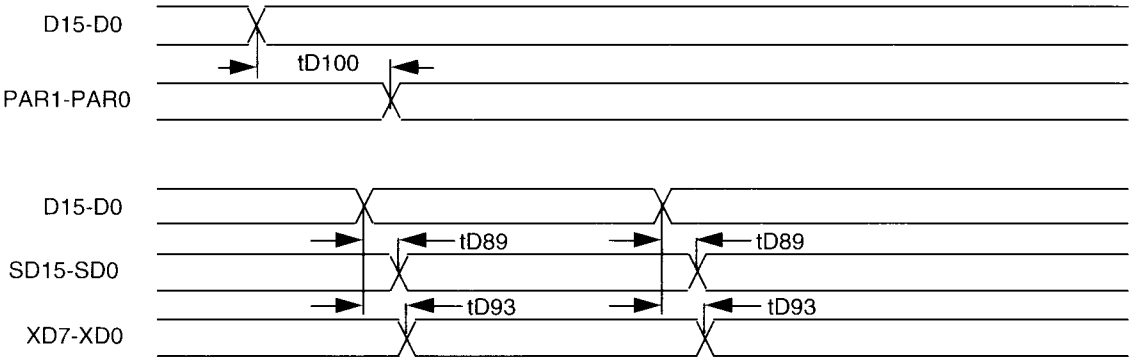


FIGURE 16. XD BUS TIMINGS

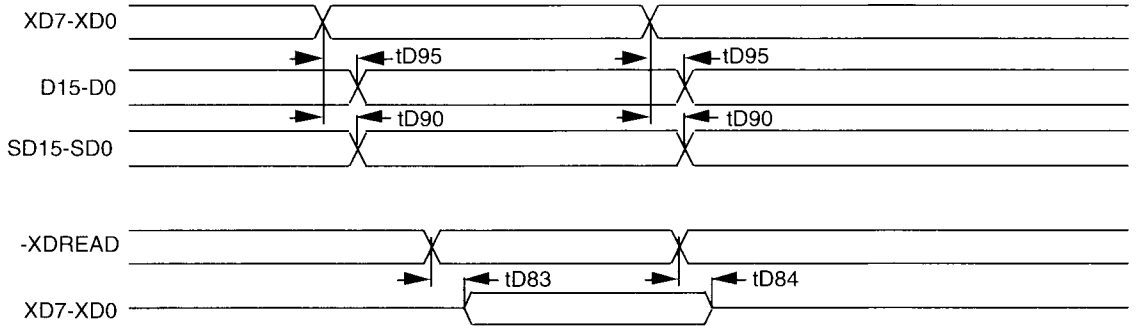


FIGURE 17. SD BUS TIMINGS

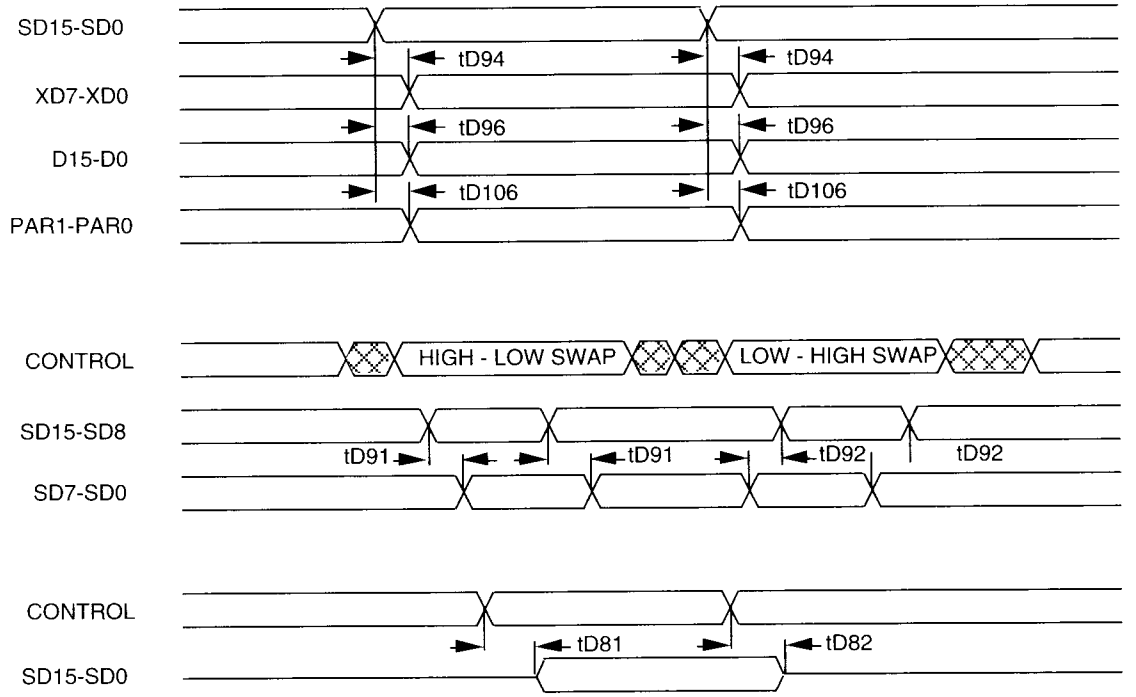
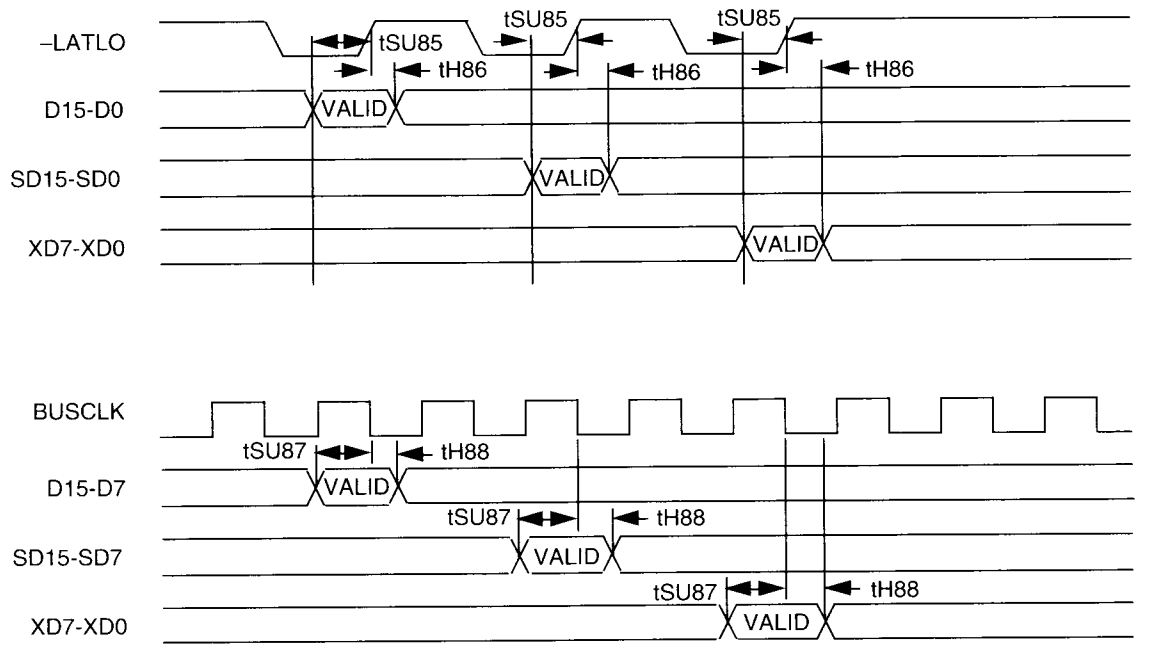


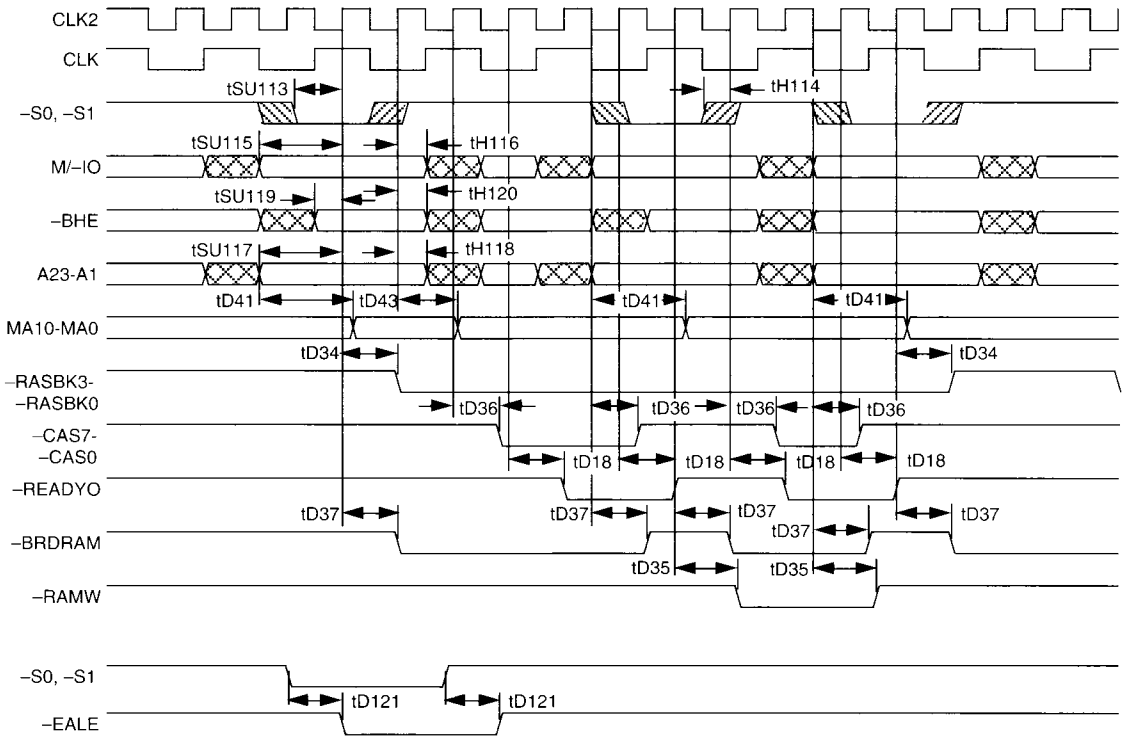
FIGURE 18. DATA LATCH TIMING



AC CHARACTERISTICS FOR 286 MODE

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	25	42	ns	
t7	CLK2IN High Time	8		ns	2.0 V
t8	CLK2IN Low Time	8		ns	2.0 V
tSU113	–S0, –S1 to CLK2IN Setup Time	17		ns	
tH114	–S0, –S1 from CLK2IN Hold Time	9		ns	
tSU115	M/–IO to CLK2IN Setup Time	28		ns	
tH116	M/–IO from CLK2IN Hold Time	9		ns	
tSU117	A23-A0 to CLK2IN Setup Time	28		ns	
tH118	A23-A0 to CLK2IN Hold Time	9		ns	
tSU119	–BHE to CLK2IN Setup Time	8		ns	
tH120	–BHE from CLK2IN Hold Time	9		ns	
tD121	–S0, –S1 to –EALE Delay	3	19	ns	CL=50 pF

FIGURE 15. 286 MODE TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground –0.5 V to 7.0 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage –0.5 V to VDD + 0.3 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	–0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD – 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD – 0.45		V	IOH = –1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD – 0.45		V	IOH = –2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, Note 3
VOH3	Output High Voltage	VDD – 0.45		V	IOH = –12 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 12 mA, MISCSET5 = 1 IOL = 24 mA, MISCSET5 = 0, Note 4
VOH4	Output High Voltage	VDD – 0.45		V	IOH = –6 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 12 mA, CTRL1[2] = 1 IOL = 24 mA, CTRL1[2] = 0, Note 5
VOH5	Output High Voltage	VDD – 0.45		V	IOH = –6 mA, Note 5
VOL6	Output Low Voltage		0.45	V	IOL = 10 mA, RAMSET7,6 = 00 IOL = 20 mA, RAMSET7,6 = 01 IOL = 30 mA, RAMSET7,6 = 10 IOL = 40 mA, RAMSET7,6 = 11, Note 6
VOH6	Output High Voltage	2.4		V	IOH = –6 mA, RAMSET7 = 0 IOH = –12 mA, RAMSET7 = 1, Note 6
VOL7	Output Low Voltage		0.45	V	IOL = 8 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOL = 24 mA, Note 8
ILI	Input Leakage Current	–10	10	µA	Note 9
IIL	Input Leakage Current	–500	10	µA	Note 10
IIH	Input Leakage Current	–10	500	µA	Note 11
ILO	Output Leakage Current	–100	100	µA	

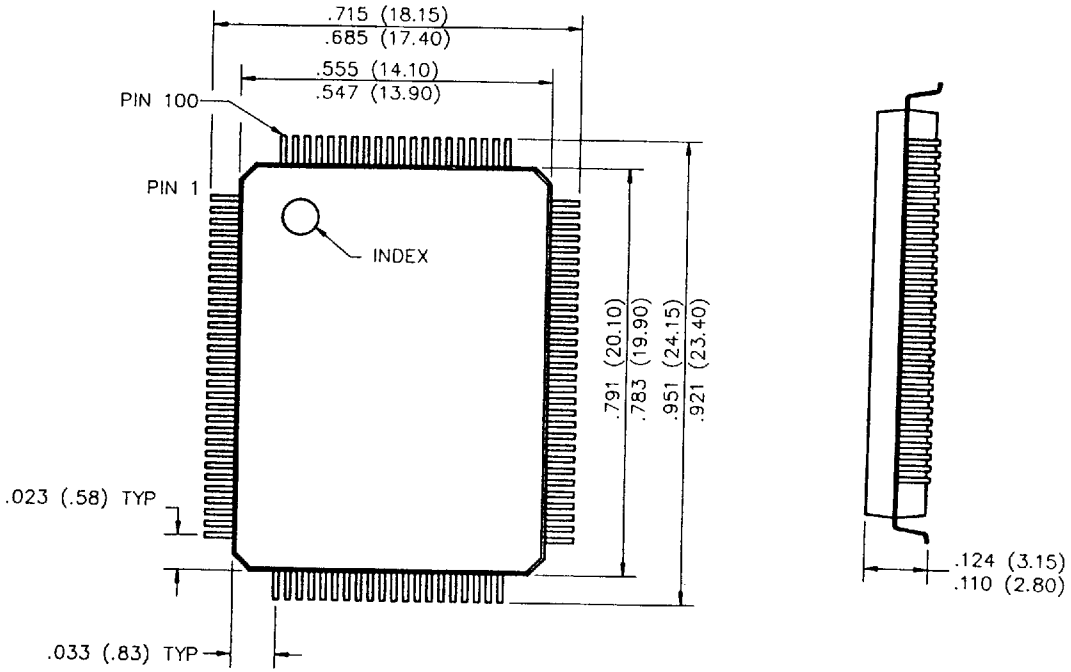
DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

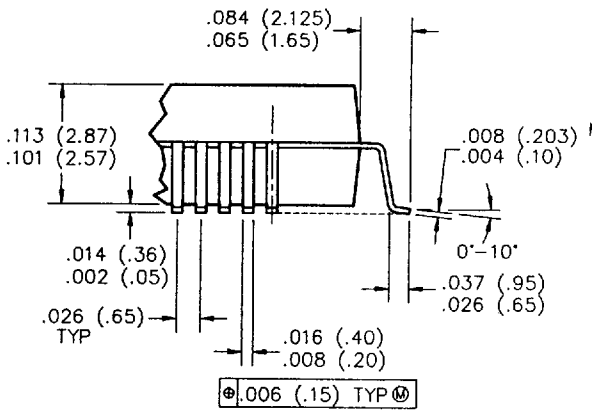
Symbol	Parameter	Min.	Max.	Unit	Conditions
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	Based on CLK2 Frequency
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	
VILTC	Input Low Voltage	–0.5	0.8	V	TCLK2 Input Levels
VIHTC	Input High Voltage	2.8	VDD + 0.5	V	TCLK2 Input Levels

Notes:
1. Pins: –BUSYCPU, PEREQCPU, –ROMCS, IRQ13, –NPCS, –PARERROR, XD7-XD0
2. Pins: –READYO, HRQ, RESCPU, D15-D0, PAR1, PAR0, –CAS7- –CAS0, RESNPX, –EALE, –BRDRAM, –CHS0/–MW, –CHS1/–MR, CHM/–IO, –BLKA20, BUSCLK, DMAHLDA
3. Pins: CLK2
4. Pins: SD15-SD0
5. Pins: –RASBK3- –RASBK0
6. Pins: MA10-MA0, –RAMW
7. Pins –SLP/MISS
8. Pins: –REFRESH
9. All inputs except those listed in notes 10 and 11
10. Pins: –ERRORNPX, –BUSYNPX, 286/–386SX, –TRI, W/–R (–S0), D/–C (–S1), M/–IO, –ADS
11. Pins: PEREQNPX

100-PIN PLASTIC QUAD FLAT PACK

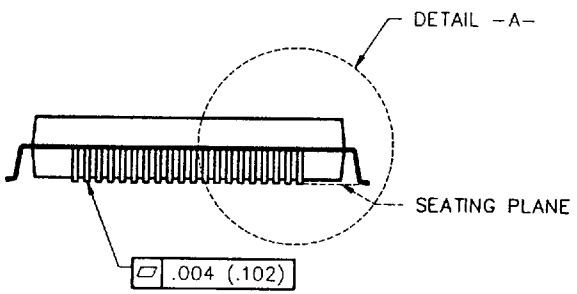
V L S I TECHNOLOGY INC





DETAIL –A–

NOTES:
1. CONTROLLING DIMENSION IS MM.



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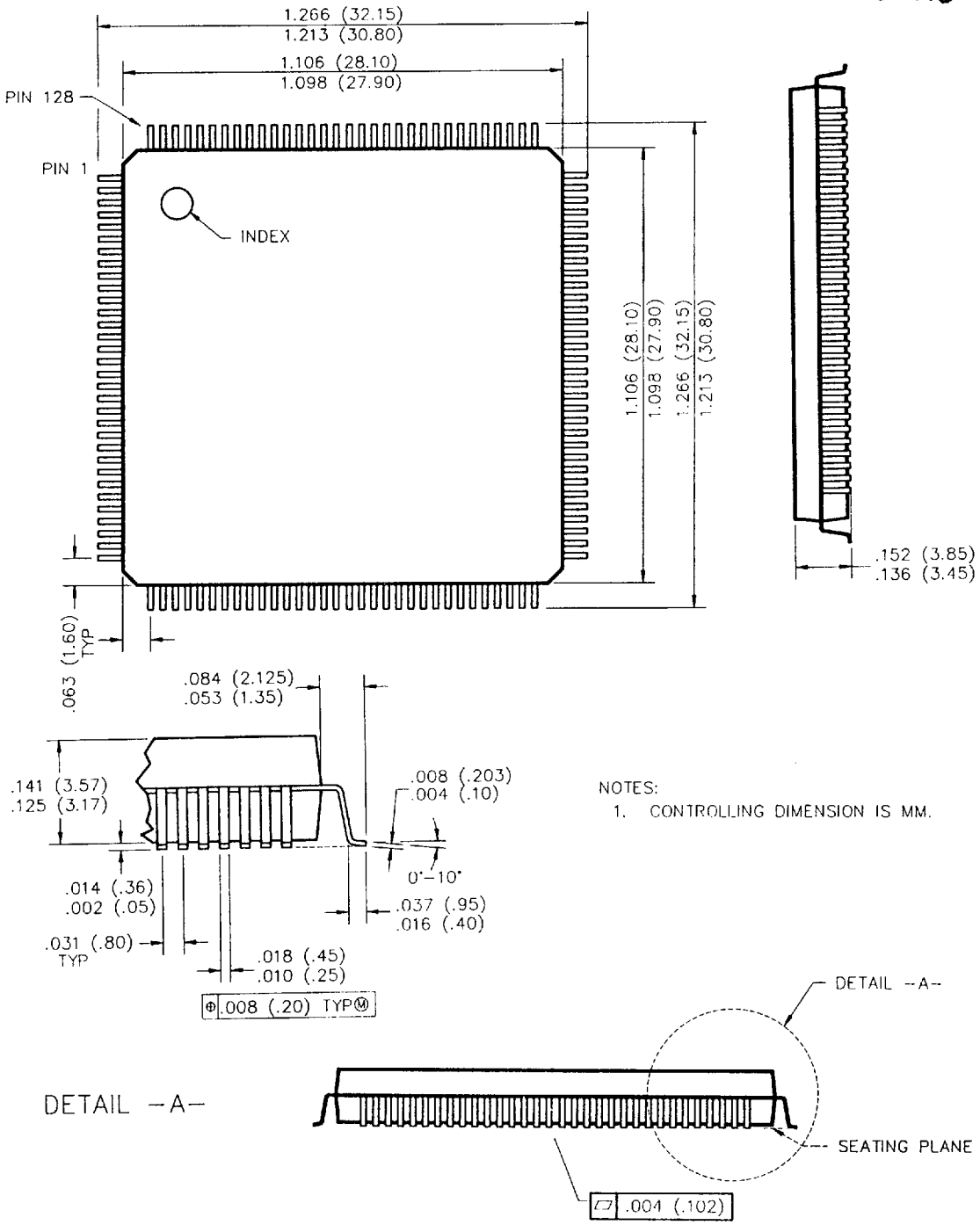
128-PIN PLASTIC FLAT PACK

V L S I TECHNOLOGY INC T-90-20

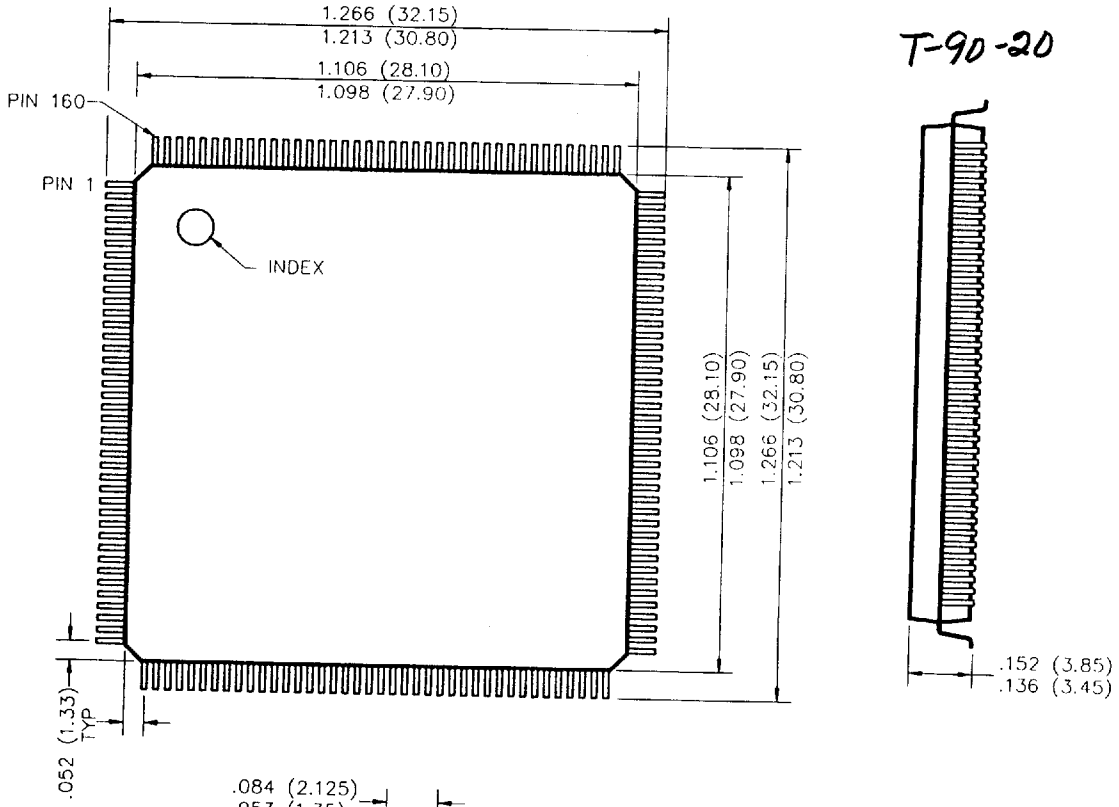


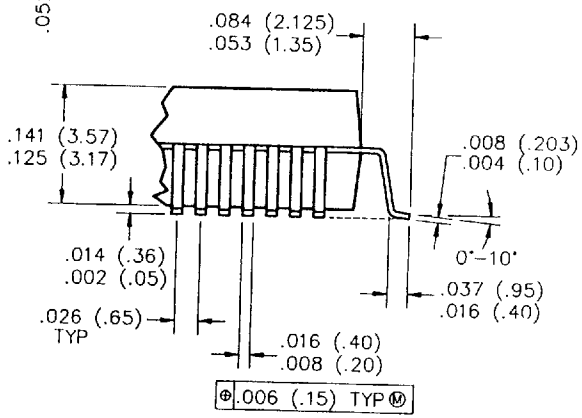
NOTES:
1. CONTROLLING DIMENSION IS MM.

160-PIN PLASTIC QUAD FLAT PACK

V L S I TECHNOLOGY INC

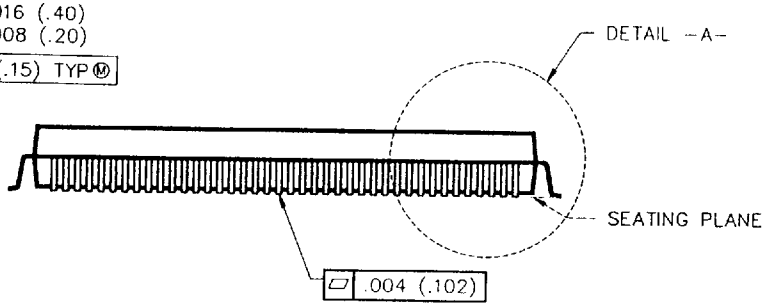
T-90-20





NOTES:
1. CONTROLLING DIMENSION IS MM.

DETAIL –A–



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